

Virtual Impedance Shaping for low voltage Microgrids

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Abstract—AC Microgrids, in presence of highly non-linear loads, require a tighter regulation of line voltage to maintain power quality. This article proposes an outer virtual impedance loop to shape the output voltage in such microgrids. In order to achieve this, a virtual impedance extracting and shaping filter is first proposed to extract and weigh selected frequency components of the line current. Secondly, design of impedances to weigh the extracted frequency components is obtained in order to achieve harmonic current sharing and reducing total harmonic distortion (THD) even in scenarios of asymmetric sharing of highly non-linear loads. An isochronous voltage-active power half droop architecture is also employed to achieve active, reactive power sharing and to keep circulating currents minimum in the low-voltage microgrid. Analytical results on designing virtual impedances and their dependence on network line parameters are obtained. Finally, MATLAB/SIMULINK-based simulations are performed on a 4.4 kVA microgrid and implemented on a low-cost controller in a controller-hardware-in-the-loop (CHIL) setup to validate the viability of implementation and efficacy of the proposed virtual impedance shaping method.

I. INTRODUCTION

AC Microgrids are becoming prevalent due to their economic and technical benefits compounded with the increased resiliency and reliability they offer [1]. However, the challenges of maintaining power quality in islanded AC microgrids require further investigation as non-linear loads are ubiquitous. Current operating standards for microgrids [2] require voltage and power quality to follow stringent limits even in the presence of such large number of non-linear loads for safe operation of the microgrid and its connected components.

Conventional droop-based approaches are not suitable for mitigating harmonic imbalances caused due to mismatches in harmonic current sharing among the various voltage source inverters (VSI) in a low-voltage (LV) microgrid with non-linear loads. These mismatches arise due to the sensitivity of the closed-loop output impedance at the VSI towards control methodology and line parameters. Virtual impedance based methods have shown promising applicability to shape the dynamic profile of the VSIs. Virtual impedance techniques have been employed for harmonic sharing and THD improvement [3], [4], [5], [6]. However, these approaches have limitations when applied to active (P), reactive (Q) and harmonic power sharing objectives. [7] proposes a reactive power disturbance input in the conventional droop law to

reduce reactive power sharing mismatch while affecting the active-power sharing accuracy and stability of the system frequency. [6] provide a signal injection method to mitigate power imbalances however, rendering additional complexities in employing this approach. Moreover, $P \sim Q$ decoupling characteristics change in LV AC microgrids with high R/X ratio. [8], [9] address the resistive output impedance but are not generalized to include complex impedances. [10] proposes an FFT-based harmonic extraction using a feed-forward loop that is highly dependent on parameter variation. [11] implements an inductive-capacitive virtual impedance but such approach can introduce unwanted resonances in the system. In [8], [9], [12] the equivalent output impedances are designed to be dominated by the virtual impedances to effectively reduce circulating currents and improving power sharing accuracy. However, line impedance mismatches are not considered. Secondary control approaches are considered in [13], [14] to improve P, Q sharing accuracy however, the centralized control strategies are complex and rely on availability of a communication network. [15] proposes a distributed apportioning method using voltage active power droop however harmonic power sharing is not considered.

In order to address these issues, a synchronous reference frame (SRF)-based harmonic extraction and shaping filter is proposed in this article for effective harmonic sharing between VSIs in an LV networks. SRF approaches show best performance under non-sinusoidal conditions if reactive-power sharing can be compensated by other means [16]. Thus, an isochronous Voltage-active power droop (VP-D) law is implemented to maintain active and reactive power sharing in the network. This implementation assumes the access to a timing signal in the microgrid for generating a frequency reference signal to the inverters such as a Global Positioning systems (GPS) receiver [17]. Advancements in GPS technology for providing timing signals and timing intervals at the accuracy of nanosecond timescales have become widely accessible and can be implemented for realizing such a microgrid. The SRF-based framework of [18], [19] is extended to achieve desired performance parameters in the system such as voltage regulation, P , Q , harmonic power sharing using nominal line parameters that can be estimated using various methods [20], [21].

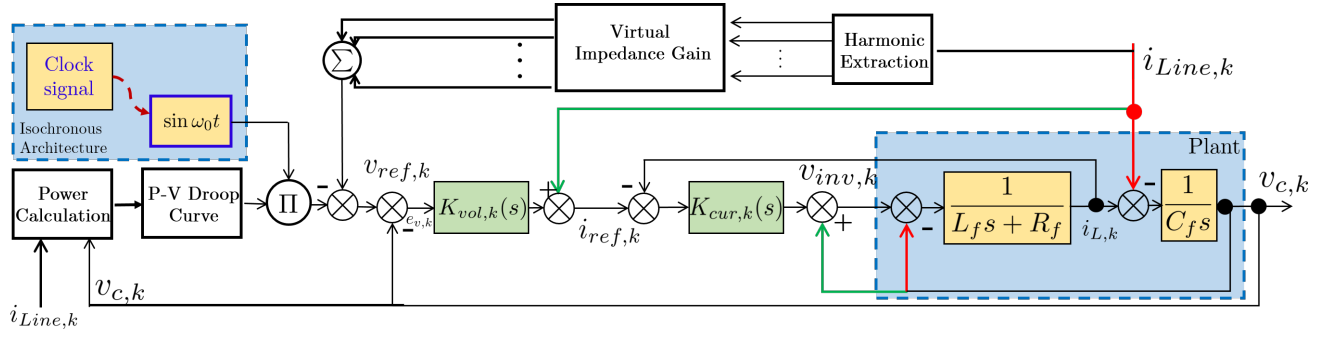


Fig. 1. Virtual Impedance shaping with inner-outer controller and Voltage-Active Power Droop architecture

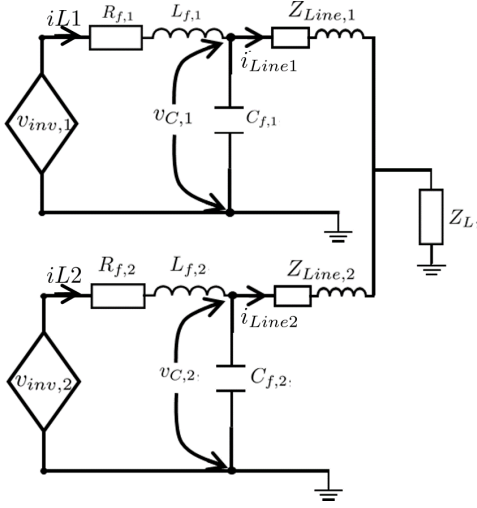


Fig. 2. Two inverter setup with voltage source inverters, line parameters and common load.

II. SYSTEM DESCRIPTION

A. Single Inverter System

The single inverter system comprises of a single-phase H-bridge inverter with an output LC-filter connected to a common load, Z_L , through a line impedance, $Z_{Line,k}$. The inverter is modeled as a controlled voltage source, $V_{inv,k}$. The dynamics of the k^{th} inverter employing average model [22] are given as:

$$V_{c,k}(s) = G_{inv,k} V_{inv,k}(s) - G_{i,k} I_{Line,k}(s) \quad (1)$$

$$\text{where } G_{inv,k} = \frac{1}{L_k C_K s^2 + R_k C_K s + 1} \text{ and } G_{i,k} = \frac{L_k s + R_k}{L_k C_K s^2 + R_k C_K s + 1}.$$

Here, $V_{c,k}(s)$ is the output voltage, $G_{inv,k}$ and $G_{i,k}$ are the transfer functions from the control input $V_{inv,k}$ to $V_{c,k}$ and $I_{Line,k}$ to $V_{c,k}$ respectively of the k^{th} VSI in laplace domain. The control design (shown in Fig. 1) is facilitated by a multi-loop controller with an outer voltage controller, $K_{vol,k}(s)$,

based on the internal model principle design of a Proportional resonant controller structure [23] and an inner current loop, $K_{cur,k}$, to be a PI controller. The proposed control law of the inverter is given as:

$$V_{inv,k} = K_{ref,k} V_{ref,k}(s) - K_{v,k} V_{c,k}(s) - K_{ref,k} Z_{v,k} I_{Line,k}(s), \quad (2)$$

where $K_{ref,k} = K_{cur,k} K_{vol,k}$, $K_{v,k} = K_{ref,k} + K_{cur,k} C_K s - 1$. The two inverter microgrid setup is shown in Fig. 2.

B. Voltage-active power droop

An *outer voltage-active power droop law* (VP-D) is employed given as, $E_k = E^* - n_k(P_k - P_k^*)$, where E_k , E^* , n_k , P_k and P_k^* are inverter and reference output voltage magnitudes, droop coefficient, measured output active power, and reference active power of the k^{th} inverter. The reference voltage to be tracked by each inverter is given by, $v_{ref,k} = E_k \sin \omega_0 t - \sum_h Z_{vhk} i_{Line,hk}$, where the time signal is obtained by an isochronous architecture to achieve accurate synchronization to a common clock. Here h denotes the harmonic number, $h = 1$ denotes the fundamental frequency component. Detailed analysis of the design of droop gains for such a system is provided in [24].

C. Isochronous Architecture

An isochronous architecture is achieved by providing a common clock signal to all the inverters in the network. The reference voltage is provided to be $v_{ref,k} = E_k \sin \omega_0 t$. The advantages of such an architecture are i) the ability to operate the microgrid at a single frequency, thereby eliminating deviation of frequency that arises while using frequency-droop control, ii) simplified control of the inverters by implementing only VP-D control without explicitly controlling reactive power and, iii) enabling a ‘plug and play’ nature of the microgrid. Note that successful synchronization with the common clock and compliance with IEEE 1588-2008 standards [25], enabling accurate and precise synchronization of the real-time clocks of the networked distributed devices to the common clock, is assumed throughout. It is imperative that such an architecture is robust to error in clock measurements or momentary loss of access to the common clock by one or more inverters in the system. Such a scenario can be mitigated

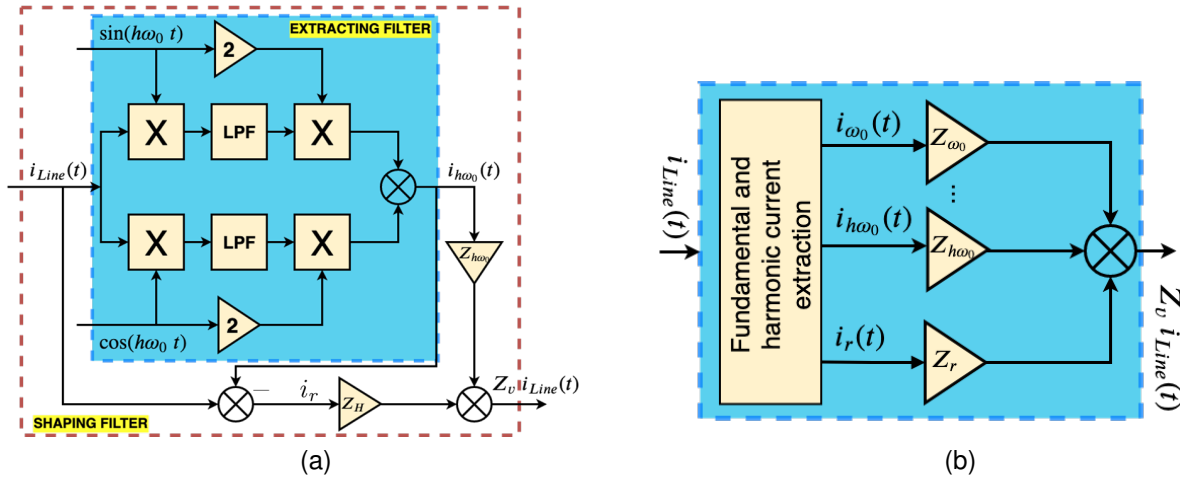


Fig. 3. (a) Virtual impedance shaping and extracting filter of k^{th} inverter line current at $h\omega_0$ rad/s, (b) series of harmonic extracting filters for obtaining shaped reference voltage for k^{th} inverter.

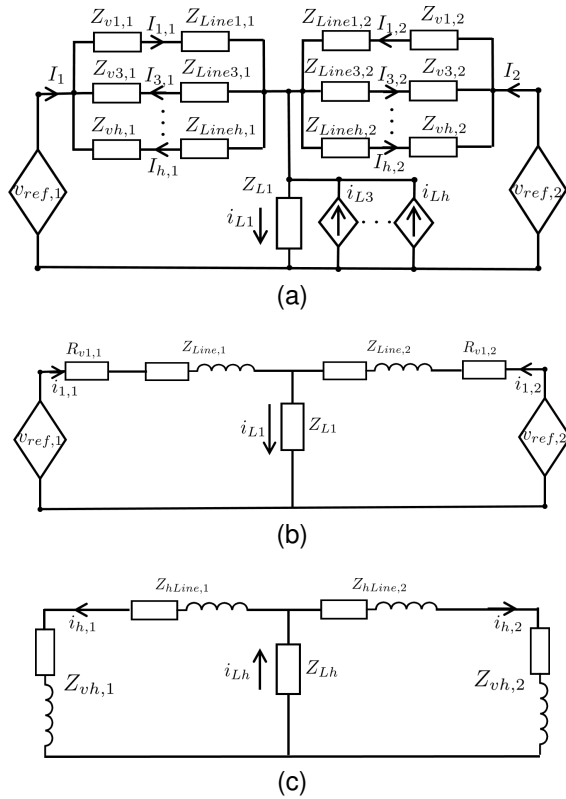


Fig. 4. (a) Equivalent circuit of a two VSI interconnection, (b) equivalent circuit in fundamental domain, (c) equivalent circuit in harmonic domain.

by employing a corrective mechanism such as, a local PLL algorithm as proposed in [26].

D. Virtual Impedance Shaping and Extracting Filter

In order to obtain the harmonic components of the line current for each VSI, a direct component and a quadrature component are extracted in the synchronous reference frame. Fig. 3a shows the shaping and extracting filter that takes

the k^{th} inverter line current, $i_{Line,k}(t)$ as input to extract the fundamental frequency component, $i_{\omega_0}(t)$ for ($h = 1$). The extracting filter receives sinusoidal modulation signals of frequency ω_0 rad/s.

Thus, the decomposition of the line current to obtain the h^{th} harmonic signal, is given as,

$$i_{h\omega_0}(t) = a_h \sin(h\omega_0 t) + b_h \cos(h\omega_0 t), \quad (3)$$

where $a_h = \frac{2}{T} \int_0^T i_{Line}(t) \sin(h\omega_0 t) dt$ and $b_h = \frac{2}{T} \int_0^T i_{Line}(t) \cos(h\omega_0 t) dt$, where T is the time-period of the periodic signal.

Remark: It is to be noted that the isochronous architecture allows for the local inverter controllers to have access to the common clock aiding in generation of modulation signals of appropriate frequency without additional complexities of implementing SRF-based phase-locked loops.

Selective harmonic components of the line current (see Fig. 3b), $i_{h\omega_0}(t)$ for $h = 3, 5, 7, \dots$, can be extracted by selecting respective harmonic modulation signals of frequency hf_0 Hz in the extracting filter in eq. (3). This approach is based on the extension of synchronous reference frame low pass filter to fundamental and harmonic frequency extraction for unbalanced nonlinear loads [18]. Virtual impedances are implemented as weighting functions to weigh the output of the extracting filters to obtain a shaped output voltage reference, given as,

$$V_{ref,k} = E_k \sin \omega_0 t - \left(Z_{\omega_0} i_{\omega_0} + \sum_{h=3,5,7,\dots} Z_{h\omega_0} i_{h\omega_0} \right)$$

III. ANALYSIS OF PROPOSED VIRTUAL IMPEDANCE SHAPING METHOD

For k^{th} inverter, the Laplace transform of line current can be expressed as,

$$I_{Line,k}(s) = \sum_{h=1,3,5,\dots} I_{Line,hk}(s) \quad (4)$$

, where $h = 1$ denotes the fundamental frequency component. substituting eq. (4) the control law given in eq. (1) and eq. (2), we get,

$$\begin{aligned} V_{c,k}(s) &= G_{inv,k}(s)V_{inv,k}(s) - G_{i,k}(s) \sum_{h=1,3,5,\dots} I_{Line,hk}(s) \\ &= G_{inv,k}(s) \left(K_{ref,k}(s)V_{ref,k}(s) - K_{v,k}(s)V_{c,k}(s) \right. \\ &\quad \left. - (K_{ref,k}(s)Z_{v,k} \sum_{h=1,3,5,\dots} I_{Line,hk}(s)) \right. \\ &\quad \left. - G_{i,k}(s) \sum_{h=1,3,5,\dots} I_{Line,hk}(s) \right) \\ &= G_{inv,k}(s) \left(K_{ref,k}(s)V_{ref,k}(s) - K_{v,k}(s)V_{c,k}(s) \right) \\ &\quad - \sum_{h=1,3,5,\dots} \left(G_{inv,k}(s)K_{ref,k}(s)Z_{vh,k}(s) \right. \\ &\quad \left. + G_{i,k}(s) \right) I_{Line,hk}(s) \end{aligned}$$

Hence, the inverter dynamics with the control law can be rewritten as,

$$V_{c,k} = G_k(s)V_{ref,k}(s) - \sum_{h=1,3,5,\dots} Z_{hk}(s)I_{Line,hk}(s), \quad (5)$$

where,

$$\begin{aligned} G_k(s) &= \frac{G_{inv,k}(s)K_{ref,k}(s)}{(1 + G_{inv,k}(s)K_{v,k}(s))}, \\ Z_{hk}(s) &= \frac{(G_{inv,k}(s)K_{ref,k}(s)Z_{vh,k} + G_{i,k}(s))}{(1 + G_{inv,k}(s)K_{v,k}(s))}. \end{aligned}$$

The analysis of eq. (5) shows that the thevenin equivalent circuit of the VSI with the proposed control law and extracting filters can be decoupled into its constituent harmonics domain (See Fig. 4a). Thus, the inverter interconnection can be analyzed in fundamental and harmonic circuits (as shown in Fig. 4b and Fig. 4c). In the harmonic domain, inverter output impedances are modeled as virtual impedances, $Z_{vh,k} = R_{v,k} + jh\omega_0 L_{v,k}$.

In order to achieve harmonic current sharing, the virtual impedance for h^{th} harmonics for inverter k can be designed

$$Z_{vh,k} + Z_{Line,hk} = Z_{tot,hk}, \quad (6)$$

for $h = 3, 5, \dots$ (Fig. 5) for a known nominal $Z_{tot,hk}$. Analysis of the harmonic domain also reveals that for the judicious choice of virtual impedances for given inverter k such that, $Z_{vh,k} = -Z_{Lineh,k}$ results in generating a reference $v_{ref,k}$ for the isochronous VP-D-based control loop that allows for maximum mitigation of harmonic drops in output voltage at point of common coupling (PCC).

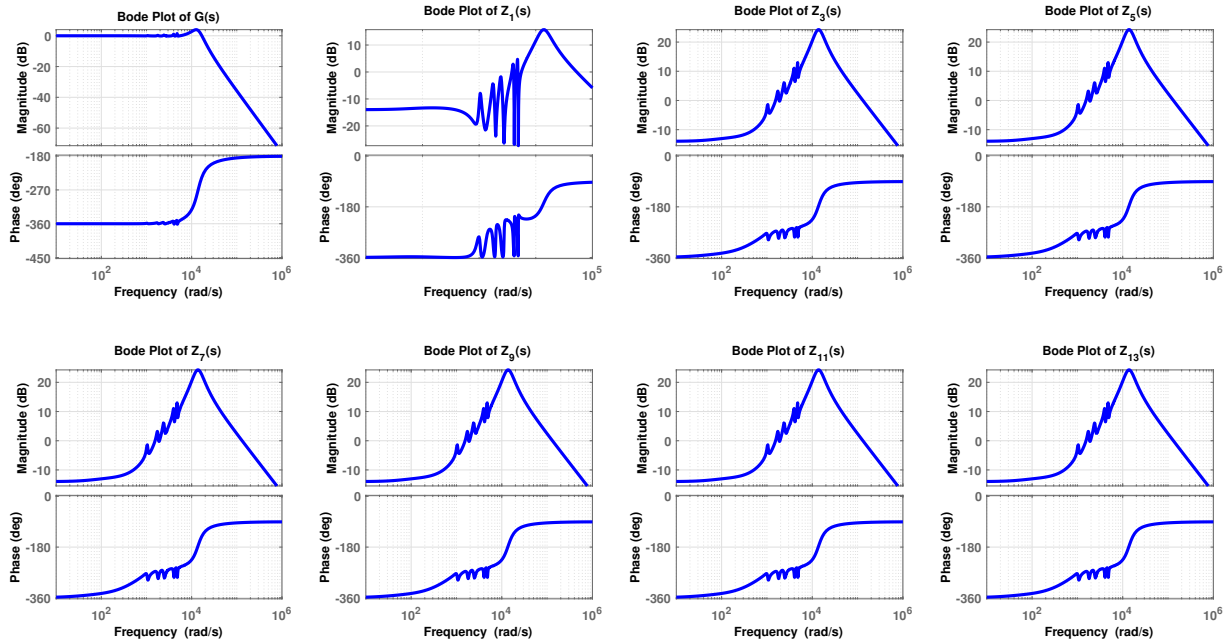


Fig. 5. Bode plots of transfer function for voltage reference tracking $G(s)$ and virtual impedance designed for harmonic current sharing ($h = 1, 3, 5, 7, 9, 11, 13$) for the two-inverter setup.

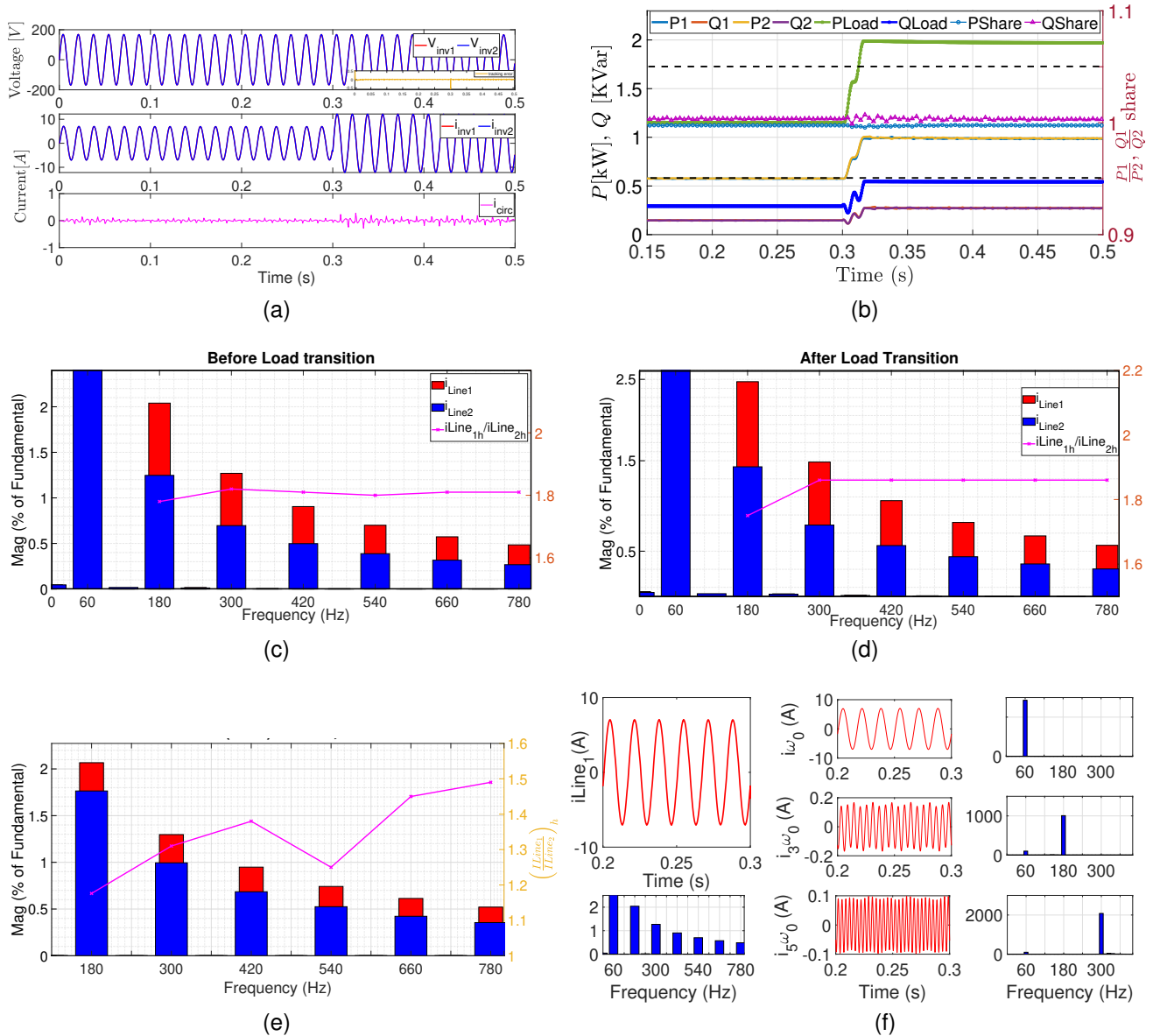


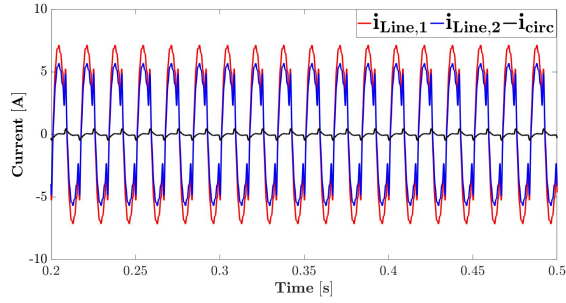
Fig. 6. (a) Performance of proposed control law for voltage tracking and reduced circulating currents; (b) active, reactive power sharing accuracy; (c) harmonic current sharing before load transition for $t < 0.3s$; (d) harmonic current sharing after load transition at $t = 0.3s$; (e) harmonic current sharing between the two VSIs without virtual impedance shaping implemented; (f) Inverter 1 Line current with harmonic content (left); extracted fundamental (i_{ω_0}), third ($i_{3\omega_0}$) and fifth ($i_{5\omega_0}$) harmonics (middle); FFT analysis of the extracted signals (right).

IV. RESULTS

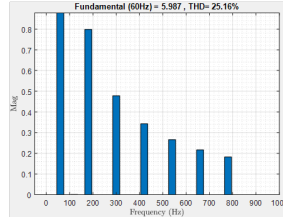
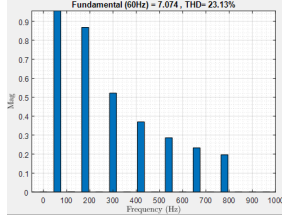
A. Simulation-based validation

SIMULINK/MATLAB simulations are performed with the setup shown in Fig. 2 with the parameters given in Table II. The two inverter system consists of VSIs of capacity 2.2kVA (1-ph, 120 V_{rms}) each implementing the proposed VP-D multi-loop controller to share active power of 1.1 kW (reactive power of 290 Var) with a load transition occurring at time $t = 0.3$ seconds to 2 kW (reactive power of 500 Var) symmetrically i.e. with an active power sharing ratio of 1 along with an increase in harmonic current demand of the load.

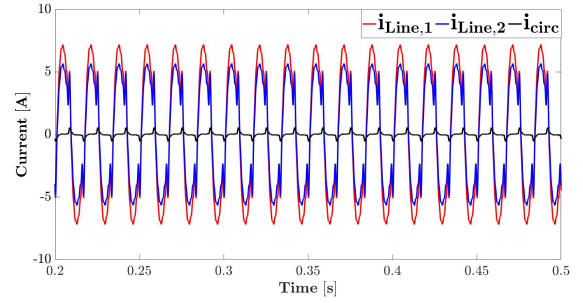
The performance of the proposed control law is shown in Fig. 6. Inverter output voltages and line currents are shown in Fig. 6a. It can be seen that the output voltages of both the inverters track the reference signal as shown by the tracking error along with the small circulating currents between the VSIs. Fig. 6b shows the active and reactive power sharing accuracy of the proposed architecture with virtual impedance design. The active power is shared by the two VSIs symmetrically as commanded by the outer droop law. It is important to note that the reactive power shared by both the VSIs are also symmetrical even when reactive power is not



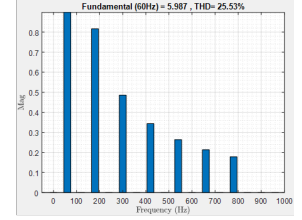
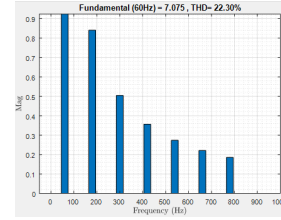
(a)



(b)



(a)



(b)

Fig. 7. Two-inverter setup results without implementing virtual impedance loop; (a) Inverter line and circulating currents, (b) FFT analysis of Inv 1 and Inv 2 output currents.

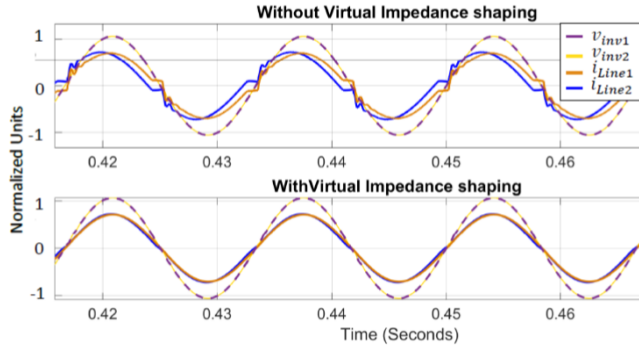
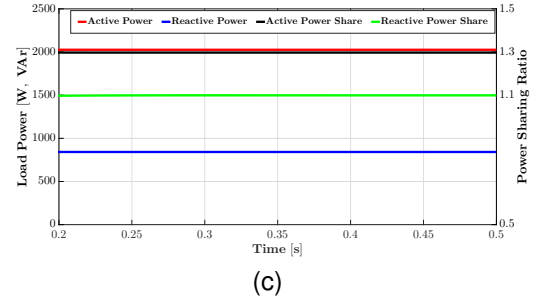


Fig. 8. Inverter output voltages and line currents for improving circulating current with virtual impedance shaping

explicitly controlled in the proposed VP-D architecture. The non-linearities in the common load, Z_L , are modeled to have a total demand distortion (TDD) of 5% in compliance with IEEE standards for allowable harmonic currents in an electric power system [27]. TDD is considered here as it is a measure of the total harmonic current distortion against the full load demand of the power system. A 13th order extracting filter is implemented for each voltage source inverter. Fig. 5 shows the bode plots of the complementary sensitivity transfer function $G(s)$ from $V_{ref}(s)$ to $V_c(s)$ as well as the output impedances Z_h for $h = 1$ to $h = 13$. The inductive component of the virtual impedance is realized by a second order generalized integrator (SOGI). The virtual impedances are designed to dominate line impedances and provide a harmonic current sharing ratio of $\left(\frac{I_{Line1}}{I_{Line1}}\right)_h = 1.82$. Results of this harmonic



(c)

Fig. 9. Two-inverter setup results with virtual impedance loop; (a) Inverter line and circulating currents, (b) FFT analysis of Inv 1 and Inv 2 output currents, (c) Active, reactive power sharing with VP-D.

sharing before and after load transition at $t = 0.3$ are shown to meet the harmonic sharing ratio ($< \pm 5\%$) in Fig. 6c and Fig. 6d respectively. For comparison, harmonic current sharing of the two inverter setup without implementing virtual impedance shaping is shown in Fig. 6e. Finally, Fig. 6f shows the efficacy of the extracting filters where the output of the filters for the fundamental (relative to DC) and harmonic number 3 and 5 for line current of inverter 1.

An asymmetric power sharing case is shown with $Z_{Line2} = 0.05\Omega + j\omega_0 0.17mH$. In this case the virtual impedances are designed to share the harmonic currents symmetrically and the active power asymmetrically with a sharing ratio of 1.3. An FFT analysis of the inverter line currents (Fig. 7b and Fig. 9b) shows the harmonic current sharing to be significantly improved as shown in Table I. Again a reactive power sharing ratio of 1.1 is maintained with the proposed VP-D architecture.

Fig. 8 shows a case where virtual impedances are designed to limit the circulating currents (and phase mismatches in line currents) between the two inverters. The virtual impedance

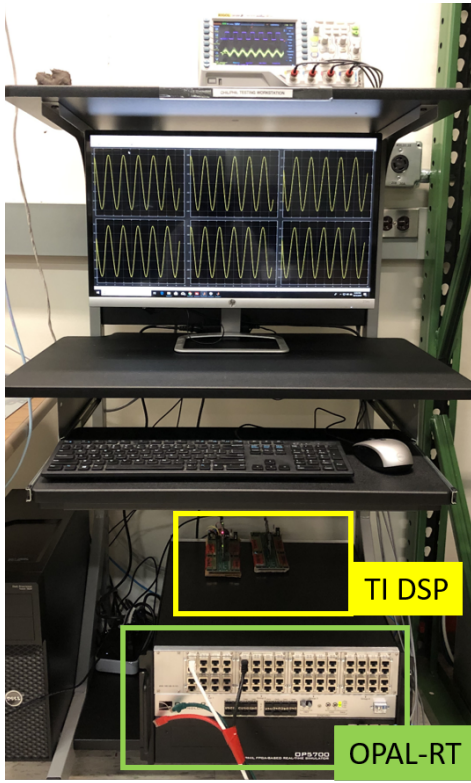


Fig. 10. Two VSI setup for CHIL-based validation on OPAL-RT with TI DSP controllers.

shaping method resulted in reducing the phase lag between the output currents of the inverters, thereby reducing circulating current from 0.75 amps to 0.38 amps. THD of PCC voltage is also improved by 64% (from 1.01 to 0.36).

TABLE I
HARMONIC CURRENT SHARING RATIO FOR CHIL

$\frac{I_{inv1,h}}{I_{inv2,h}}$	Without Virtual Impedance shaping	With Virtual Impedance Shaping
h=3	0.35	1.02
h=5	1.41	1.06
h=7	1.39	1.03
h=9	0.41	1.03
h=11	0.41	1.045
h=13	0.41	1.00

B. CHIL validation

Controller-hardware-in-the-loop(CHIL)-based validations are performed for the two VSI-setup along with the parameters shown in Table II where the two line impedances are unequal. The CHIL setup (Fig. 10) consists of external TI DSP F28379D (delfino) micro-controller units to implement the proposed VIS method and demonstrate its applicability for real-world low cost embedded controllers. Discretized shaping and extracting filters are implemented and the results are shown in Fig. 11 through Fig. 13 with VIS implementation to achieve equal harmonic sharing (≈ 1.05). The CHIL

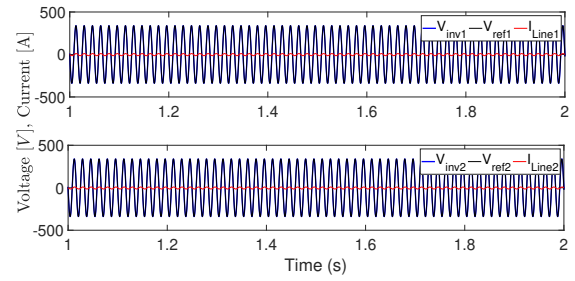


Fig. 11. Performance of the proposed control of VIS units in CHIL simulations.

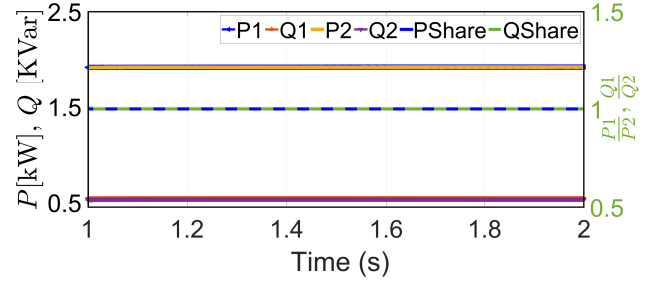


Fig. 12. Active, reactive power sharing accuracy with VP-D in CHIL simulations.

simulation also validates accuracy of active and reactive power sharing to be close to 1 with the proposed VP-D control.

V. CONCLUSION

This article proposes and demonstrates the design and implementation of a virtual impedance shaping method for low-voltage AC microgrids. An SRF-based extracting filter is proposed for extracting fundamental and selective harmonic components of inverter line currents and virtual impedances, implemented as weighing filters, are designed based on one or more performance parameters of the microgrid system such as symmetric or asymmetric harmonic current sharing. An isochronous voltage-active power droop law is proposed to maintain active and reactive power sharing by providing VSIs access to a time clock/interval signal. Analysis of the design

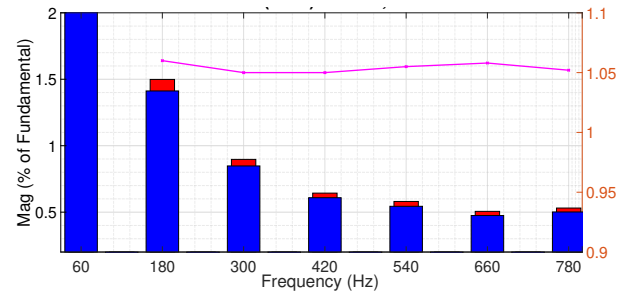


Fig. 13. Harmonic sharing performance in CHIL simulations for the two VSI system.

TABLE II
SIMULATION PARAMETERS

Parameters	Values
Nominal Frequency at PCC ($f_o = \frac{\omega_o}{2\pi}$)	60 Hz
Rated Power of Inverter ₁	2.2 kVA
Rated Power of Inverter ₂	2.2 kVA
Extracting Filter Order	13
Parameters for MATLAB/SIMULINK simulations	
Nominal Voltage at PCC (E^*)	120√2 V
R-L Load	2 kW/ 1 kVAR (5 % TDD)
Z_{Line1}	$0.19\Omega + jh\omega_0 0.1\text{mH}$
Z_{Line2}	$0.2\Omega + jh\omega_0 0.17\text{mH}$
Parameters for CHIL experiments	
Nominal Voltage at PCC (E^*)	240√2 V
R-L Load	4 kW / 1 kVAR (5 % TDD)
Z_{Line1}	$0.02\Omega + jh\omega_0 0.05\text{mH}$
Z_{Line2}	$0.01\Omega + jh\omega_0 0.08\text{mH}$
Z_{Tot}	$0.04\Omega + jh\omega_0 0.1\text{mH}$

of virtual impedances are provided for LV microgrids. Finally, validations are obtained through SIMULINK/MATLAB simulations as well as CHIL-based real time simulation on a two inverter set-up to demonstrate the performance of the proposed methodology when implemented on low cost micro-controller devices.

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