

Isochronous Architecture-Based Voltage-Active Power Droop for Multi-Inverter Systems

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Abstract—This article proposes an isochronous architecture for parallel inverters with only voltage-active power droop (VP-D) control for improving active power sharing as well as plug-and-play of multi-inverter-based distributed energy resources (DERs). The isochronous framework obviates the need for an explicit regulation of the frequency while allowing for sharing of reactive power. The article demonstrates that the detrimental effects of circulating currents between inverters can be addressed in the framework developed. The isochronous architecture is implemented by employing a GPS to disseminate clock timing signals that enable the microgrid to maintain the nominal system frequency. Small signal eigenvalue analysis of a Multi-inverter Microgrid system near the steady-state operating point is presented to evaluate the system stability. Moreover, unlike traditional droop-based methods, the isochronous strategy lends itself to analytical guarantees which are developed in the article. Furthermore, the effect of delays in receiving GPS clock signals by an inverter is experimentally characterized and an inverter isolation mechanism is proposed that disconnects inverters facing large GPS communication delays. Hardware experiments on an 1.2 kVA-prototype and controller-hardware-in-the-loop validation on the CIGRE distribution network are conducted to demonstrate the effectiveness of the proposed architecture towards active and reactive power sharing between inverters with various load scenarios.

Index Terms—Common-clock/GPS, low-voltage multi-inverter microgrid, virtual impedance, voltage active power droop.

I. INTRODUCTION

MODERNIZATION of rapidly dispatchable DERs to provide demand response and ancillary services are

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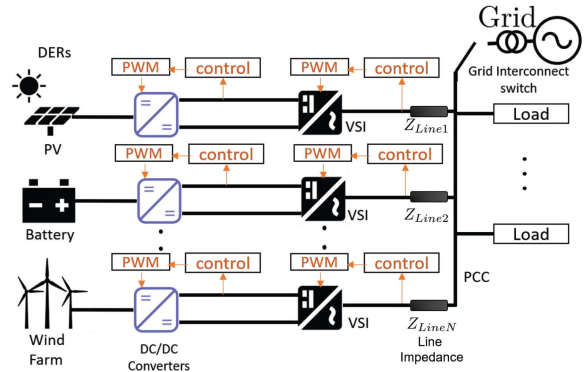


Fig. 1. Microgrid with DERs interfaced with DC/DC converters and VSIs with control, to regulate voltage and frequency at PCC and power sharing between DERs, terminated at AC loads.

transforming emergent microgrids into advanced microgrids enabling additional flexibility, resilience and reliability for local resources as well as support of the large scale grid when connected [1]. These multi-inverter microgrids (MMGs) [2] are systems that allow interaction of various DERs such as photovoltaics (PV) and battery energy storage systems connected to loads with DC/DC converters and DC/AC inverters (referred to as voltage source inverters (VSIs)) at the point of common coupling (PCC) as shown in Fig. 1. MMGs can be operated in both grid-connected as well as islanded modes. In the islanded mode, DERs support local loads in the microgrid through either centralized, distributed or de-centralized control architectures. Such controllers are employed either locally at individual DERs or at the microgrid level and are responsible for, stabilizing microgrid voltage [3], [4], maintaining power quality [5] with plug-and-play capabilities [6], apportioning load between various distributed generations (DGs) [7], and primary frequency response support [8]–[10]. However, control of VSIs in MMGs pose the additional challenge of regulating system frequency and output voltage in the absence of a stiff grid. Furthermore, these VSIs need to be controlled such that the DERs share the load demand, satisfying active and reactive power requirements according to a prescribed sharing ratio. High performance in meeting these objectives are difficult to achieve due to the uncertainty in load demand size and load schedules, and, due to the complexity that arises as a result of the coupling of paralleled VSIs in an MMG.

A distributed and communication-less approach of controlling VSIs is typically achieved through droop control methods.

These methods use measurements obtained locally at the DERs and leverage the relationships between system voltage, line frequency, and power supplied by the DERs to ensure regulation of voltage and frequency in the network [11]. In microgrids with high line inductance (high X/R ratio), DERs are generally controlled by conventional $P - f$ and $Q - V$ droop control [12], [13], where P , Q , f , and V are active power, reactive power, frequency, and voltage respectively. The droop strategies in microgrids are motivated by the autonomous control of synchronous generators, with large rotating inertia directly coupled with the network that primarily rely on conventional droop strategies for regulation of system voltage and frequency. However, low voltage (LV) microgrids use more converter-interfaced DERs, and thus, exhibit low natural inertia with significant R/X ratio because of the small spatial expanse of the networks [14]. Consequently, non-conventional $P - V$ and $Q - f$ droop control strategies [14], [15] have gained attention for LV microgrids with the advantages of direct voltage control [16] and improved harmonic power sharing [17] compared to conventional droop control. Moreover, in order to improve transient performance and leverage decoupling compensations for droop controlled MMG, there are several works in the literature concentrating on modifying the droop characteristic equations [18]–[22]. However, these more complicated droop characteristic equations are, difficult to analyze, give stability guarantees, and difficult to incorporate in applications.

In traditional full droop based strategies that employ a frequency related droop strategy ($P - f$ or $Q - f$), the droop laws are designed to allow participating DERs to agree upon a system frequency based on the operating conditions and the specified droop curves. As a result, deviation of microgrid system frequency from nominal is inevitable. In the case of LV microgrids that have low inertia due to converter-interfaced DERs, the system frequency may deviate considerably from nominal [12], [23], [24]. In order to mitigate the detrimental effects of large excursions in frequency, typically, a secondary controller is employed that utilizes communication between DERs to restore the steady state system frequency to nominal [25]; however, complete mitigation of transient frequency deviations caused by sudden load changes in islanded microgrids is not achieved. Frequency regulation becomes even more difficult in the presence of uncertain renewable energy resources. Furthermore, traditional full droop methods suffer from the fundamental limitation of the trade-offs between accurate power sharing on one hand and the desire for stringent regulation of system voltage and frequency on the other.

An alternative to traditional full droop strategies is to adopt a half-droop strategy where only the system voltage is regulated based on the changes of active power while keeping the system frequency constant by utilizing intelligent communication technologies such as GPS-based timing signals [26]. Reference [27] presents a decentralized control method for meshed microgrids to allow plug-and-play of DERs. However, additional measurements are required that render such strategies difficult and expensive to implement. A power-angle droop strategy is proposed in [24] to allow DERs to share the power demand based on the voltage angles. However,

one drawback of this approach is the slow dynamic response because of delays in measuring power and obtaining voltage angles. A local rotating reference frame based synchronization using GPS timing signals is proposed in [28] to synchronize DERs utilizing the direct and quadrature-axis components of the reference voltage and output current which involve additional computations that can be avoided in single phase MMGs. Similarly, [29] proposes an augmented strategy where the GPS timing signal is used in conjunction with an adaptive $Q - f$ droop characteristics as a backup to ensure stable operation of the microgrid during GPS interruptions. Reference [29] uses a voltage-current droop law for maintaining active power sharing whereas in this article the active-power and voltage coupling of LV microgrids is used for controlling active power sharing.

In this article, we propose using only VP-D control for voltage regulation and address frequency regulation by providing a common timing signal from a GPS receiver to all the inverters. The framework developed enables generation of a common frequency reference for all the inverters and avoids the need for explicit frequency control and obviates the need for communication between inverters. Conventionally, $P - V/Q - f$ droop characteristics results in an inevitable deviation in system frequency as a result of which the designed controllers are affected if the system frequency is off-nominal due to the $Q - f$ droop characteristics. A GPS based isochronous VP-D half droop controller allows the system frequency to be always maintained at nominal thereby resulting in a better decoupling of the active and reactive power control. Moreover, the half-droop is easier to implement on low cost controller devices due to reduced complexity of the controller design. Additionally, the dependence of VSI output voltage and current on network parameters such as droop gains, line parameters can be obtained analytically, in closed-form, that allows for better design of the controllers for MMGs and provides insights on the effect of various parameters on the stability and performance.

In contrast to existing GPS-based methods [27], [29], our approach simultaneously achieves multiple objectives including reduced circulating currents between VSIs with better voltage regulation, reduced complexity due to the absence of phase locked loops (PLL) required for frequency synchronization and plug-and-play of VSIs. The main contributions of the proposed isochronous architecture are summarized as follows.

- 1) Access to common clock pulses in this architecture enables operation of the Multi-inverter Microgrid (MMG) at a single frequency even in the presence of system disturbances. VP-D control decouples voltage regulation objectives from frequency variations thereby alleviating issues such as frequency dependent control resulting in poor voltage regulation and poor disturbance rejection. The architecture also enables improved start up transients, reduced circulating currents between participating VSIs and easy plug-and-play of VSIs in the MMG.

- 2) The architecture does away with issues stemming from active frequency-regulation in full-droop methods. VP-D control allows direct control of active power with regulation of voltage magnitude. The resulting control law guarantees that

the parallel inverters share reactive power such that deviations from desired reactive power sharing remain bounded while serving a common load even without explicitly controlling the reactive power flow. The resulting controller design is simpler as no explicit $Q-f$ control is required.

3) The proposed framework facilitates a comprehensive analysis that provides: i) delineation analytically of how circulating current between VSIs depends on output voltage regulation error; ii) small-signal based stability analysis of the ac microgrid by having access to the common clock signal to generate $\alpha-\beta$ components without added complexities of PLL dynamics. These provide useful design guidelines for selecting droop gains and virtual output resistances to maintain system stability.

4) A VSI isolation mechanism is proposed to allow VSIs to detect locally, delays in GPS signals (with respect to a tolerance value) and the ability to disconnect from the MMG. The resulting flexibility in provides delay tolerance based on performance requirements of the MMG. Furthermore, the effect of GPS communication delays on MMG is studied experimentally and characterization of time delay is obtained for the operational stability of the MMG.

Results show that the proposed architecture exhibits improved transients over full-droop implementations during start-up and different plug-and-play scenarios. Accuracy of active power and reactive power sharing is observed to improve whereas circulating currents among inverters greatly reduced. Moreover, the transient response time to reach steady state improved in proposed VP-D architecture when compared to full-droop control. Moreover, the proposed VP-D control exhibits tighter regulation of the PCC voltage regulation during plug-and-play of the MMG system. Experimental results are provided for a system of two 0.6 kVA inverters under different load variations and sharing ratios to validate the feasibility and effectiveness of the proposed isochronous architecture.

The rest of the article is organized as follows. Section II describes the system and control architecture. Section III provides analytical results for the multi-inverter system, and Section IV presents simulation, experimental validation on a two-inverter microgrid network and CHIL experiments on the CIGRE distribution network. The effect of delay in receiving GPS signals and an inverter isolation mechanism are also proposed in this section. Finally, Section V summarizes observations and insights that highlight this work.

II. SYSTEM DESCRIPTION AND CONTROLLER DESIGN

This section provides the details of an LV resistive MMG network containing N parallel VSIs, serving a common load, Z_L , connected at a single point of common coupling (PCC) as shown in Fig. 2. Each inverter in the MMG includes a communication module that receives synchronized clock pulses from the GPS segment [30] through a GPS receiver. These clock pulses are then used by the proposed outer VP-D control to provide a synchronized sinusoidal reference voltage signal to inner-loop controllers located at each VSI forming the isochronous system architecture. We begin our discussion by describing first the dynamics of the k^{th} single inverter

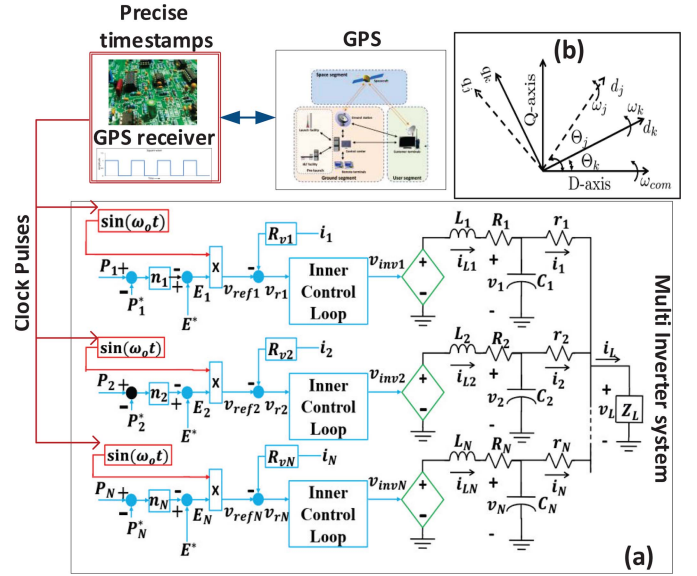


Fig. 2. (a) A parallel N -inverter MMG with outer-droop and inner multi-loop controllers receiving GPS signals [30] to disseminate clock signals for frequency regulation, (b) representation of VSI j and VSI k with respect to common reference frame.

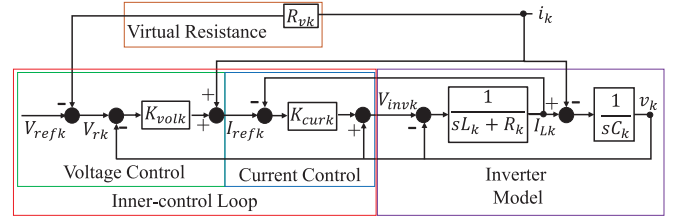


Fig. 3. The inner-control loop for voltage regulation with a virtual resistance.

system and the controllers employing the proposed control law for achieving output voltage regulation and load disturbance rejection through a cascaded multi-loop control architecture.

A. Single Inverter System With Multi-Loop Control Design

A single phase H-bridge inverter with an output LC filter is connected to load Z_L through a line resistance r_k . The VSI is modeled as a controllable voltage source, V_{invk} , by employing an average model of the inverter [31]. The dynamics of the k^{th} VSI are described as:

$$L_k \frac{di_{Lk}}{dt} + R_k i_{Lk} = v_{invk} - v_k, \quad C_k \frac{dv_k}{dt} = i_{Lk} - i_k$$

where v_{invk} , i_{Lk} , v_k , and i_k are average values over one switching cycle (T_s) of control signal, inductor current, output voltage, and output current, respectively (See Fig. 3). Taking Laplace transforms and eliminating $I_{Lk}(s)$, we get,

$$V_k(s) = \frac{1}{L_k C_k s^2 + R_k C_k s + 1} V_{invk}(s) - \frac{(L_k s + R_k)}{L_k C_k s^2 + R_k C_k s + 1} I_k(s). \quad (1)$$

The control design objectives are to: i) regulate the output voltage of the inverter (V_k) to track a reference signal (V_{rk}); ii) regulate the output inductor current of the inverter (I_{Lk}) to track a reference signal (I_{refk}); iii) reject disturbances due to load variations. We propose the following control law:

$$V_{invk}(s) = K_{refk}V_{refk}(s) - K_{vk}V_k(s) + K_{ik}I_k(s), \quad (2)$$

where $K_{refk} = K_{curk}K_{volk}$, $K_{vk} = K_{refk} + K_{curk}sC_k - 1$, and $K_{ik} = -K_{refk}R_{vk}$. As shown in Fig. 3, the control law takes the form of cascaded voltage and current controllers. The outer voltage controller, K_{volk} , acts on a sinusoidal reference signal provided by the outer droop law with the incorporation of a voltage drop, $i_k R_{vk}$, on a virtual resistance, R_{vk} . A feed-forward of the line current, i_k is used to minimize inrush currents and improve the transient response of the outer voltage controller. The output of the voltage controller, I_{refk} , provides the sinusoidal reference current signal to be tracked by the inductor current which generates the controllable voltage signal, V_{invk} , for the k^{th} VSI. The main advantages of the inner-outer loop structure are the decoupled design of the fast inner current controller and the slow outer voltage controller as well as the increased robustness of the VSI to load variations. By combining (1) and (2), the closed-loop averaged output voltage dynamics of k^{th} inverter are given by:

$$V_k(s) = G_k(V_{refk}(s) - R_{vk}I_k(s))(s) - Z_kI_k(s), \quad (3)$$

where $G_k = S_k G_{v_{invk}} K_{refk}$, $S_k = (1 + G_{v_{invk}} K_{vk})^{-1}$ is the sensitivity transfer function, $T_k = 1 - S_k$ is the complementary transfer function, and $Z_k(s) = S_k G_{ik}$. Note that, $Z_k(j\omega_0) := (1 + G_{v_{invk}} K_{vk})^{-1} G_{ik}|_{s=j\omega_0}$ is the equivalent Thevenin output impedance of the k^{th} inverter at the fundamental frequency, $\omega_0 = 2\pi 60$ rad/s. The primary control objectives thus translate to $G_k(j\omega_0) \approx 1$ for voltage regulation and the closed-loop inner- current loop transfer function from I_{refk} to I_{Lk} be such that $T_{I_{refk} \rightarrow I_{Lk}}(j\omega_0) \approx 1$ and $Z_k(j\omega_0) \ll 1$. The current-control and voltage-control designs are based on the internal model principle [31], [32], where the controllers K_{curk} and K_{volk} are designed to have poles $s = \pm j\omega_0$ and loop-shaping-based design to cancel the pole located at $s = R_k/L_k$ by the current controller. Moreover, the design ensures proper separation in bandwidth of both the controllers (current control loop has the larger bandwidth), which enables the inner current loop to make the inductor current I_{Lk} to track the reference current I_{refk} .

An output virtual resistance loop [17] is also adopted to alleviate the sensitivity of active power sharing to the line and output impedances. Here, the virtual resistance, R_{vk} , is designed to dominate the line impedance of the k^{th} VSI, rendering the design insensitive to line and filter parameters. However, R_{vk} is bounded above to ensure VSI output voltage regulation to be within prescribed limits as larger R_{vk} results in larger regulation error by reducing V_{rk} . When we need to emphasize the fundamental frequency, ω_0 , we make the following assumption.

Assumption 1: In Fig. 3 the following conditions are met:

- 1) $v_{refk}(t)$ and $i_k(t)$ are sinusoidal with frequency ω_0 .
- 2) $K_{volk}(s)$ has poles at $\pm j\omega_0$. ($\frac{1}{s^2 + \omega_0^2}$ is a factor.)

- 3) The closed-loop system from reference voltage, $v_{rk}(s)$, to output voltage, $v_k(s)$, is stable.

The following theorem shows that if all external inputs (i.e., $v_{refk}(t)$ and $i_k(t)$) to the system are sinusoidal with frequency ω_0 , then the inverter voltage follows the sinusoidal reference $v_{rk}(t)$ with zero steady-state error.

Theorem 1: Under Assumption 1, the closed loop system in steady state satisfies,

$$v_k(t) = v_{rk}(t) = v_{refk}(t) - R_{vk}i_k(t).$$

Furthermore, $G_k(j\omega_0) = 1$ and $Z_k(j\omega_0) = R_{vk}$ in (3).

Proof: See Appendix. ■

The theorem above establishes the performance of the proposed VP-D controller towards regulation of output voltage and disturbance rejection of output line current for an inverter at the nominal frequency.

B. Outer Voltage-Active Power Droop

The sinusoidal voltage reference signal, $V_{refk}(s)$, used by the inner multi-loop controllers is generated by the proposed VP-D control law. The proposed droop law does not facilitate any explicit control on reactive power (Q) unlike full droop control methodologies where active and reactive power are controlled separately by controlling voltage and frequency respectively. The VP-D law for the k^{th} VSI is

$$E_k = E^* - n_k(P_k - P_k^*), \quad (4)$$

where E_k , E^* , n_k , P_k , and P_k^* are inverter output voltage magnitude, reference output voltage magnitude, droop coefficient, measured output active power, and reference active power of the k^{th} inverter. Here, $v_{refk}(t) = E_k \sin(\omega_0 t)$. To control E_k , it is necessary to measure P_k which is usually achieved by measuring instantaneous power (i.e., $p_k = v_k(t)i_k(t)$) and passing it through a first order low pass filter (LPF) with bandwidth ω_P which is designed to be much smaller than the voltage control loop. Reference [33], a preliminary version of the results in this article, obtains a near-exact solution for determining the active power for a single VSI serving a load.

C. Full Droop Architecture

In AC microgrid during *islanded* mode, grid-forming VSIs are operated in voltage control mode to perform the tasks of regulating the PCC voltage and frequency. Level 1 or primary control of the microgrid provides the reference voltage and frequency set point to the controllers of grid-forming VSIs. These control methods are usually implemented either by using the communication-based active load sharing techniques or by mimicking the droop characteristics of a conventional synchronous generator system followed for multiple interconnected synchronous machines. The common droop characteristics used for multiple interconnected synchronous machine-based system use linear dependence slopes for the i^{th} unit as n_i and m_i selected as:

$$n_i = \frac{f_{NL} - f_{FL}}{P_{FL,i}}, \quad (5a)$$

$$m_i = \frac{V_{NL} - V_{FL}}{Q_{FL,i}}, \quad (5b)$$

where, f_{NL} , V_{NL} and f_{FL} , V_{FL} are the steady-state frequency and RMS voltage of the system at no-load and full-load respectively. $P_{FL,i}$ and $Q_{FL,i}$ are the full-load active and reactive power capacity of i^{th} unit. For both frequency-active power and voltage-reactive power droop it can be shown that the active and reactive power sharing ratio among generating units can be controlled by properly choosing the slope of the characteristics.

Chandorkar *et al.* [34] first proposed the droop characteristic-based independent, autonomous, and wireless control of multiple VSIs by eliminating the inter-communication links between them. The droop characteristic equations for VSIs used in [34] are as follows:

$$\omega = \omega^* - n_i(P_i - P_i^*), \quad (6a)$$

$$V = V^* - m_i(Q_i - Q_i^*), \quad (6b)$$

where, ω^* , V^* are nominal system frequency (in rad/sec) and nominal system voltage (RMS) respectively. P_i^* , Q_i^* are active and reactive power reference set-points respectively of the i^{th} VSI. n_i and m_i are the corresponding droop coefficients and P_i and Q_i are output active and reactive power outputs of i^{th} VSI.

In [34], the droop characteristic-based control is directly adapted for multiple VSIs in an islanded microgrid by mimicking the interconnected synchronous machine case. However, the behavior of droop-control in an islanded microgrid is complex where its precise and accurate operation rely significantly on the VSI control techniques, its parameters and microgrid network parameters.

D. GPS as Timing Signals

Apart from providing navigational data, GPS systems can provide accurate clock signals for civilian usage via the Standard Positioning Service (SPS). SPS is available for civilian use and has an accuracy of 340 ns. GPS-SPS satellite signals contain digitally modulated information in the carrier wave and the GPS signal contains clock pulse data. GPS receivers can compare the clock pulses received from the GPS satellite m and compare it to a local clock to obtain a time difference, which we denote as $\Delta\tau_m$ [26]. Inherent clock biases, C_b , are always present due to deviations in local clock and GPS clock. At any given instant the coordinates of GPS satellite m are known, we can determine the spatial position of the receiver (user) and the clock bias uniquely, with signals from four different GPS satellites, given as the solution to:

$$(x_m - x_r)^2 + (y_m - y_r)^2 + (z_m - z_r)^2 = (c\Delta\tau_m - C_b)^2,$$

where $[x_m, y_m, z_m]$ for $m = \{1, 2, 3, 4\}$ are the x , y and z coordinates of the four satellites at any given time, c is the speed of light and $[x_r, y_r, z_r]$ are the spatial coordinates of the receiver. If C_b is known then receiver (in this case a VSI) can accurately obtain universal coordinated time (UTC) required to synchronize with the accurate universal clock. GPS is used to obtain absolute time, time interval and frequency with precision up to hundred of nanosecond (ns) [30]. Low cost GPS modules can obtain time-stamping even triggers to about 50 nanosecond accuracy in Coordinated Universal Time (UTC) between widely separated sites [35]. GPS receiver modules

have the ability to measure high precision timing signals which are readily available and inexpensive making them an ideal candidate for time synchronization applications. We emulate low-cost Raspberry-Pis as GPS receiver modules (described in detail in Section IV) to receive timing signals from an emulated GPS. It is assumed here that there is accurate and precise synchronization of the real-time clocks of the networked distributed devices to the common clock and is compliant with IEEE 1588-2008 standards [36].

E. Isochronous Architecture

An isochronous architecture can be achieved by providing a common timing signal from the GPS-SPS to all VSIs in the network. Based on the position of the VSI receiver, each VSI can thus determine its clock bias, C_b , and thereby obtain timing pulses with high accuracy. The advantages of such an architecture over frequency droop are delineated earlier in this article.

It is imperative that such an architecture be robust to any momentary loss of access to the common clock by one or more inverters in the system. Mitigation of such scenarios can be achieved by employing a corrective mechanism, for example by employing a local clock at each VSI for satisfactory operation. This is possible since a local clock can provide a reasonable estimate of GPS time signal, eventually shifting the operating point in response to load changes causing degradation in power system performance. For conditions of continued signal loss, the VSI unit cannot participate in system wide load sharing and should be isolated from the rest of the system. A radio reference signal is used in [37] in order to mitigate system wide loss of GPS reference signal. Similarly, [38] utilizes three different PLL structures to guarantee robustness versus delay or loss in communication to synchronize the phase and the frequency of all of the devices connected to the microgrid.

In order to mitigate the uncertainty in GPS communication, a VSI isolation mechanism is also proposed to allow VSIs to detect locally, delays in GPS signals (with respect to a tolerance value) along with the ability to disconnect from the MMG to maintain operational stability of the system. This article, however, mainly focuses on analyzing and obtaining system performance guarantees assuming clock synchronization is reasonably maintained at all times.

III. MULTI-INVERTER SYSTEM ISOCHRONOUS OPERATION

A. Performance of Individual Inverters

In this section, the performance of the multi-inverter system with the proposed VP-D approach is analyzed. A benefit of the VP-D approach is that reactive power sharing among individual inverters is maintained within a bound without having control of reactive power explicitly defined as a control objective. Theorem 2 provides analytical expressions for output voltage and line currents of networked VSI units.

Theorem 2: If the conditions of Assumption 1 hold, then for any complex load Z_L for the network shown in Fig. 2, the steady-state voltage and current at the output of the k^{th} inverter are, respectively, $v_k(t) = V_k \sin(\omega_0 t + \psi_k)$ and $i_k(t) =$

$I_k \sin(\omega_0 t + \phi_k)$, where,

$$I_k = \frac{\gamma_k}{r_k + R_{vk}} \sum_{m=1}^N \frac{E_m}{r_m + R_{vm}}, \quad \tan \phi_k = \frac{\sin \angle \alpha}{\cos \angle \alpha - \frac{\beta_k}{|\alpha|}}$$

$$V_k = \sqrt{(E_k - R_{vk} I_k)^2 + (R_{vk} I_k)^2}, \quad \tan \psi_k = \frac{\sin \phi_k}{\cos \phi_k - \frac{E_k}{R_{vk} I_k}}$$

where, $\alpha^{-1} = \frac{Z_L^{-1}}{\sum_m (r_m + R_{vm})^{-1}},$

$$\gamma_k = \sqrt{(\beta_k - |\alpha| \cos \angle \alpha)^2 + |\alpha|^2 \sin^2 \angle \alpha}, \quad \beta_k = E_k (\sum_{m=1}^N E_m (r_m + R_{vm})^{-1})^{-1}.$$

Proof: See Appendix. ■

Corollary 1: In the case of purely resistive load, i.e., $Z_L = R_L$, the steady state voltage and current at the output of the k^{th} inverter are $v_k(t) = V_k \sin \omega_0 t$ and $i_k(t) = I_k \sin \omega_0 t$ for $V_k, I_k \in \mathbb{R}_+$. In other words, phase lags $\phi_k = \psi_k = 0$.

Proof: From the expression of α in Theorem 2, it can be clearly stated that if $Z_L = R_L$, then α is a pure real number and thus $\angle \alpha = 0$. Therefore,

$$\tan \phi_k = 0 \implies \phi_k = 0 \implies \tan \psi_k = 0 \implies \psi_k = 0. \quad \blacksquare$$

Remark 1: One of the outcomes of Theorem 2 and Corollary 1 is that with the assumed control architecture and without any explicit control of reactive power, there will be no extraneous reactive power flows if the load is purely resistive. This also holds true when there is an active power mismatch. This is validated and elaborated in Section IV-B and Fig. 11(a).

Remark 2: It is important to note that Theorem 2 provides analytical expressions of output current and output voltage of a single VSI when connected to an MMG. The direct dependence on line parameters, virtual impedance parameters and regulation of voltage at PCC is evident; such analytical insights are difficult to obtain in the conventional architecture. This forms the basis for designing parameters to largely improve active power sharing between VSIs. This is validated in Section IV-C.

B. Design Guideline for Droop Coefficients

In the following theorem the phase difference between inverter currents i_k and i_j is characterized in the general setting for complex linear loads.

Theorem 3: Let $\delta_k = \frac{E_k - E^*}{E^*}$, $\delta = (\delta_1 \dots \delta_N)^T$, $\lambda_v := (\frac{1}{r_1 + Z_v} \dots \frac{1}{r_N + Z_v})^T$, $\xi = \frac{\lambda_v}{\lambda_v^T \mathbf{1}}$, $v = \frac{Z_L \lambda_v^T \mathbf{1}}{1 + Z_L \lambda_v^T \mathbf{1}}$. Suppose the conditions of Assumption 1 hold, then the phase ϕ_k of i_k differs from the phase ϕ_j of i_j according to:

$$\tan(\phi_k - \phi_j) = \frac{\text{Im}(v) \frac{\delta_k - \delta_j}{1 + \xi^T \delta}}{\left(\text{Re}(v) - \frac{1 + \delta_k}{(1 + \xi^T \delta)} \right) \left(\text{Re}(v) - \frac{1 + \delta_j}{(1 + \xi^T \delta)} \right) + \text{Im}^2(v)}.$$

Proof: See Appendix. ■

Remark 3: For purely resistive load, $\tan(\phi_k - \phi_j) = 0$ as v becomes real which also follows from Corollary 1.

Remark 4: Theorem 3 can be extended to show that to ensure the phase difference in the inverter currents to be small, the values E_k have to be close to E^* . Indeed, for the phase

TABLE I
STATES OF THE MULTI-INVERTER SYSTEM

Parameters	States
Droop & LPF	P_k
Voltage Controller	$\phi_{k,dq}$
Current Controller	$\gamma_{k,dq}$
LC filter	$i_{Lk,dq}, v_{k,dq}$
Line parameters	$i_{k,dq}$
Load, Z_L	$i_{Load,DQ}$

difference of the currents to be smaller than $\epsilon \ll 1$, it follows that $|\delta_k - \delta_j| \leq \epsilon \frac{\sum_m \frac{1}{r_m + Z_v}}{|Z_L| \sin \theta_L}$ needs to be satisfied, where $\cos \theta_L$ is the p.f. of the load, Z_L .

Remark 5: The expression for δ_k depends only on E_k , whereas all other parameters are load and network parameters. Moreover, the deviation of E_k from E^* is dictated by the outer droop law. Thus, this analysis aids the appropriate choice of n_k and the allowable mismatch from the reference active power P_k^* that is to be delivered, for example., selecting droop gains n_i, n_j for any two inverters i, j , such that $n_i(P_i^* - P_i) = n_j(P_j^* - P_j)$ will keep reactive power flows in check.

Remark 6: Theorem 3 shows that for any two inverters j, k , the phase difference between inverter output currents i_j and i_k is related to the tightness of the output voltage regulation with regard to the reference voltage which also provides practical guidelines for designing the droop control.

C. Stability Analysis

One of the important aspects to be investigated for the multi-inverter system operation is its stability. The non-linear multi-inverter closed-loop system can be represented as, $\dot{X}(t) = f(X(t), u(t))$, where $X(t)$ denotes states of the system including both physical variables and internal control variables as shown in Table I and the input to the system, $u(t)$ is $v_{PCC}(t)$. The objective is to develop a small signal model of the multi-inverter system by linearizing the above system around a stable operating point. We consider the $d_k - q_k$ axis as the local reference frame for the k^{th} VSI operating at a rotating frequency ω_k . The individual VSI state equations are derived in terms of their individual local reference frame. The local reference frames are transformed to the global reference (D-Q) frame which is chosen to be the PCC reference frame operating at ω_{com} . This allows for generalizing the VP-D architecture beyond single-phase microgrids. We first consider the state equations of individual VSIs in their local reference frames represented by $\Theta_k := \theta_{com} - \theta_k$, where θ_{com} represents the synchronous reference frame angle at PCC and θ_k represents the deviation of the k^{th} VSI from the synchronous reference frame (Fig. 2(b)). The translation between local $d_k - q_k$ frame to global D-Q frame is given by,

$$T_{\Theta_k} = \begin{bmatrix} \cos \Theta_k & -\sin \Theta_k \\ \sin \Theta_k & \cos \Theta_k \end{bmatrix},$$

$$v_{kdq} = [v_{kd} \ v_{kq}]^T, \quad i_{kdq} = [i_{kd} \ i_{kq}]^T, \quad i_{Lkdq} = [i_{Lkd} \ i_{Lkq}]^T,$$

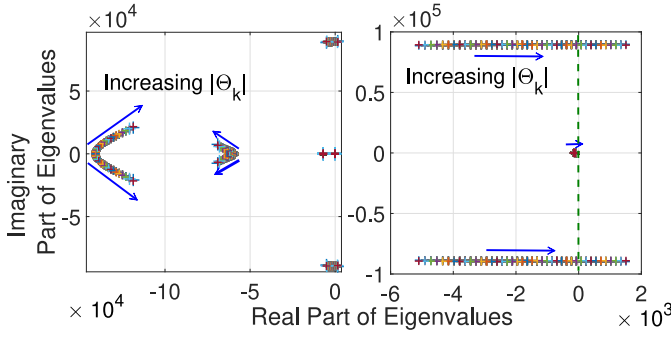


Fig. 4. Eigenvalues of the two inverter network for stability analysis with δ_k changing from 0° to $\pm 10^\circ$ for a resistive load.

where, $\begin{bmatrix} x_{kd} \\ x_{kq} \end{bmatrix} = T_{\Theta_k} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix}$. x_α and x_β are the α - β components

of a given state x . For the single phase case, $x_\beta = 0$. Note that in the case of perfect synchronization with the GPS clock signal, $\theta_k = 0$ for all VSI as a result of which all inverters can be represented in the reference frame eliminating the need for translating each VSI's states into the common reference frame. Each of these VSI units comprise an outermost droop control, inner multi-loop voltage and current controllers, output LC-filter connected to the PCC through line impedances and are terminated at the common load. Combining these dynamics, the small signal state space model of the k^{th} single inverter system is given as,

$$\Delta \dot{X}_k = A_k \Delta X_k + B_k T_{\Theta_k}^{-1} \Delta V_{PCCDQ} \quad (7)$$

where $\Delta X_k = [\Delta P_k \ \Delta \phi_{kdq} \ \Delta \gamma_{kdq} \ \Delta i_{Lkdq} \ \Delta v_{kdq} \ \Delta i_{kdq}]^T$,

Combined model of the N inverter system can now be written as [39], [40],

$$\Delta \dot{X} = \mathbf{A} \Delta X + \mathbf{B} \Delta V_{PCC,DQ}, \quad (8)$$

where $\Delta X = [\Delta X_1 \ \Delta X_2 \ \dots \ \Delta X_N]^T$, $\mathbf{A} = \text{diag}(A_1, A_2, \dots, A_N)$ and $\mathbf{B} = [B_1 T_{\Theta_1}^{-1} B_2 T_{\Theta_2}^{-1} \dots B_N T_{\Theta_N}^{-1}]^T$. Considering the dynamics of the lumped complex (Z_L) load and considering only a resistive load for simplicity, we obtain:

$$\Delta V_{PCC,DQ} = \sum_{k=1}^N T_{\Theta_k} \Delta i_{kdq} R_L \quad (9)$$

Thus, using (9) in (8) we get, $\Delta \dot{X} = \underbrace{(\mathbf{A} + R_L \mathbf{B} \mathbf{T}_\Theta)}_{\mathbf{A}_{sys}} \Delta X$,

where, $\mathbf{T}_\Theta$ is a matrix that captures the coupling of VSI interconnection at PCC. Stability analysis in the presence of a complex $R-L$ load can be obtained in a similar manner.

The stability analysis of the system is given by the eigenvalues of $\mathbf{A}_{sys}$. For a two inverter setup the eigenvalues of the system are shown in Fig. 4 setup configured with the parameters of Table III. The results are obtained for the case of an asymmetric power sharing ratio of 2.2. The line parameters are chosen to be $\text{Line}_1 = 0.2 \ \Omega + j\omega_o \ 0.1 \ \text{mH}$ and $\text{Line}_2 = 0.2 \ \Omega + j\omega_o \ 0.15 \ \text{mH}$.

TABLE II
ACTIVE AND REACTIVE POWER SHARE

Droop Coefficients (V/kW)	Line Resistance (Ω)	P_{Inv1} (kW)	P_{Inv2} (kW)	Q_{Inv1} (kVar)	Q_{Inv2} (kVar)	$\frac{Q_{Inv1}}{Q_{Inv2}}$
$n_1 = 0.025$ $n_2 = 0.025$	$r_1 = 0.10$ $r_2 = 0.10$	0.403	0.397	0.304	0.294	1.030
$n_1 = 0.025$ $n_2 = 0.016$	$r_1 = 0.10$ $r_2 = 0.10$	0.475	0.317	0.300	0.291	1.032
$n_1 = 0.025$ $n_2 = 0.025$	$r_1 = 0.10$ $r_2 = 0.09$	0.398	0.397	0.297	0.297	1.000
$n_1 = 0.025$ $n_2 = 0.016$	$r_1 = 0.10$ $r_2 = 0.09$	0.416	0.378	0.296	0.297	0.999
$n_1 = 0.025$ $n_2 = 0.025$	$r_1 = 0.10$ $r_2 = 0.08$	0.394	0.401	0.292	0.302	0.966
$n_1 = 0.025$ $n_2 = 0.016$	$r_1 = 0.10$ $r_2 = 0.08$	0.411	0.383	0.292	0.302	0.966
$n_1 = 0.025$ $n_2 = 0.025$	$r_1 = 0.10$ $r_2 = 0.07$	0.390	0.405	0.287	0.307	0.935
$n_1 = 0.025$ $n_2 = 0.016$	$r_1 = 0.10$ $r_2 = 0.07$	0.407	0.387	0.287	0.307	0.935
$n_1 = 0.025$ $n_2 = 0.025$	$r_1 = 0.10$ $r_2 = 0.06$	0.386	0.409	0.282	0.313	0.902
$n_1 = 0.025$ $n_2 = 0.016$	$r_1 = 0.10$ $r_2 = 0.06$	0.403	0.391	0.281	0.312	0.900
$n_1 = 0.025$ $n_2 = 0.025$	$r_1 = 0.10$ $r_2 = 0.05$	0.382	0.413	0.276	0.318	0.868
$n_1 = 0.025$ $n_2 = 0.016$	$r_1 = 0.10$ $r_2 = 0.05$	0.398	0.396	0.276	0.318	0.868
$n_1 = 0.025$ $n_2 = 0.025$	$r_1 = 0.10$ $r_2 = 0.01$	0.364	0.431	0.252	0.343	0.735
$n_1 = 0.025$ $n_2 = 0.016$	$r_1 = 0.10$ $r_2 = 0.01$	0.433	0.359	0.258	0.332	0.775

Remark 7: The small signal stability analysis reveals that the stability of the system is maintained in the VP-D architecture when deviation, θ_k , for all individual VSI units with respect to the common reference frame are $\leq \pm 5^\circ$. The presence of larger inductive loads (low p.f.) results in driving the eigenvalues of the linearized system towards the origin.

IV. RESULTS

A. Simulation Results

To validate the viability of VP-D-based control of a multi-inverter system, a MATLAB/SIMULINK-based switching model of two inverters sharing a common load at PCC in a LV resistive network is simulated. The network and inverter parameters used in the simulation are listed in Table III. Fig. 5 shows the voltage and current output results from a simulation where two parallel inverters are serving a common load of 0.58 kVA with $p.f. = 0.9$ (lagging). Both inverters are operated with $n_1 P_{inv1}^* = n_2 P_{inv2}^* = 2.5$ and $P_{inv1}^* = P_{inv2}^* = 250 \text{ W}$. Fig. 5(a) shows that the P share between two inverters, i.e., P_{inv1}/P_{inv2} , is maintained at 1.07. Note here that without having a separate Q control strategy, the reactive power sharing between the inverters is nearly even. Here, Q_{inv1}/Q_{inv2} is 0.88. The mismatch between actual measured and reference output active power for both the inverters, primarily because of finite line losses, results in a small voltage deviation from E^* (around -0.5%) at the PCC. The voltage waveform at the PCC and the output current are shown in Fig. 5(b). Fig. 5(c) shows the circulating current between the two inverters, which is significantly low compared to the rated output current.

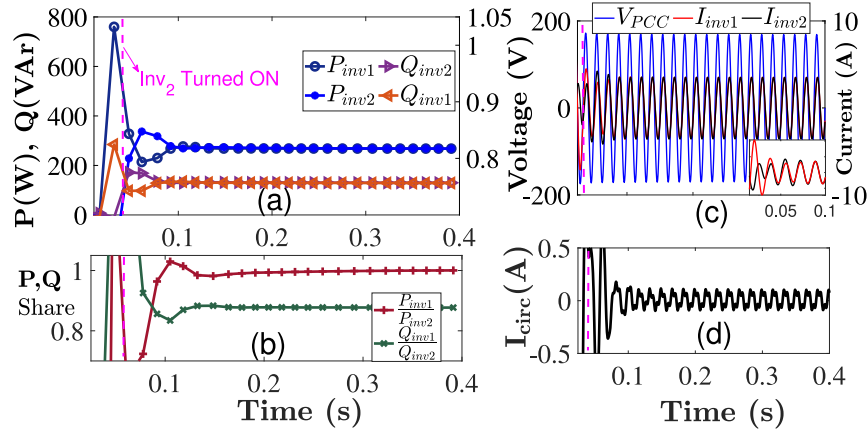


Fig. 5. Simulation results of (a) P - Q share, (b) P , Q sharing ratio, (c) voltage at the PCC and inverter output currents, and (c) circulating current between two parallel inverters.

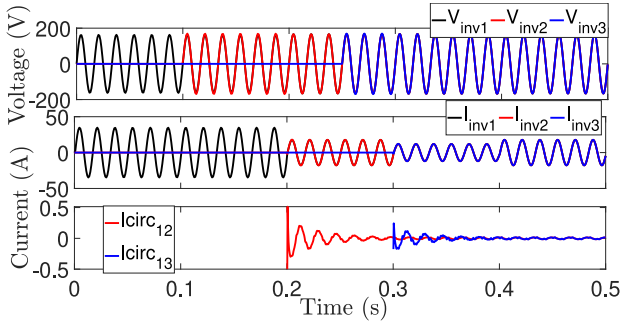


Fig. 6. MMG with VP-D for demonstrating plug and play.

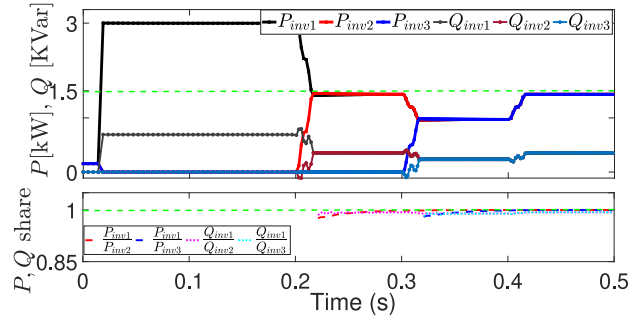


Fig. 7. P - Q sharing performance for the MMG with VP-D.

1) *Mismatched Line Parameters*: Table. II. depicts simulation results for active and reactive power sharing between two inverters employing VP-D control when active power reference values for outer droop laws are mismatched from actual active power injected by the two inverters. A number of scenarios are considered each for symmetric and asymmetric active power sharing where total reference power commanded from each inverter is $P_{inv1}^* = P_{inv2}^* = 0.6$ kW whereas the actual load, Z_L , is a series R - L load with $R = 11.52 \Omega$ and $L = 0.02293$ H. $R_v = 0.2 \Omega$ for both inverters. Results clearly showcase that the reactive power share is $0.9 \leq \frac{Q_{inv1}}{Q_{inv2}} \leq 1.03$, when the line resistance of inverter 2, satisfies $60\%r_{k1} \leq r_{k2} \leq r_{k1}$. For the cases when the line resistances are highly mismatched (i.e., $r_{k2} = 50\%r_{k1}$), $\frac{Q_{inv1}}{Q_{inv2}}$, is 0.868 with a worst-case sharing ratio of 0.735 obtained when $r_{k2} = 10\%r_{k1}$. This result demonstrates the performance of the proposed architecture in worse-case conditions toward mismatches in active power references and line parameters as equal reactive power sharing is desirable between the inverters.

2) *Plug-and-Play Capability*: A three VSI network is considered. At $t = 0$ s VSI-1 is on and synchronized with the local clock signal serving a load, $Z_L = 3$ kW (0.97 pf lagging). At $t = 0.1$ s and $t = 0.25$ s, VSI-2 and VSI-3 set individual clock receive flags high respectively to receive synchronized clock pulses for reference generation. The output voltages at the capacitor of VSI-2 and VSI-3 are thus generated at these instants. In order to demonstrate the plug and play capability, VSI-2 is connected to the common load and VSI-1 at

$t = 0.2$ s and VSI-3 is then connected to the rest of the network at $t = 0.3$ s. Symmetric power sharing is desired at all VSIs. Output voltages, line currents and circulating currents are shown in Fig. 6. Fig. 7 shows the symmetric sharing of the load, Z_L , with active power sharing ratio of 1 as well as reactive power sharing ratio of > 0.95 at steady state even when no Q control is implemented. Finally, at $t = 0.4$ s, a load transition to 4.5 kW (0.97 p.f.lagging) occurs.

3) *Comparison With Full Droop ($P - V/Q - f$)*: The three VSI network as above is considered while implementing a full droop architecture with $P - V$ and $Q - f$ droop laws. The multi-loop controller structure is designed to effectively achieve control objectives as described in Section II A, with the same P sharing objective, network parameters and common load to derive a fair comparison with the proposed architecture. At $t = 0$ s VSI-1 is on and serving a load, $Z_L = 3$ kW (0.97 pf lagging). At $t = 0.1$ s and $t = 0.3$ s, VSI-2 and VSI-3 are synchronized and connected to the network. The presence of an integrator in the $Q - f$ droop implementation results in initial transients in output voltage and current of the VSIs that cause in higher transient and steady state circulating currents. This is apparent at $t = 0.1$ s and $t = 0.3$ s when the VSIs are turned on (see Fig. 8). At $t = 0.4$ s, a load transition to 4.5 kW (0.97 p.f.lagging) occurs. The full droop implementation also suffers from longer transient times to reach steady state in both active and reactive power sharing as well as poor reactive power sharing ratio (sharing ratio of 1 is desired) during load changes and steady state

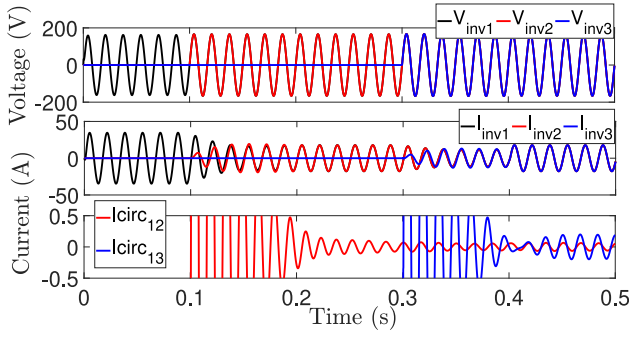


Fig. 8. MMG with full droop for demonstrating plug and play.

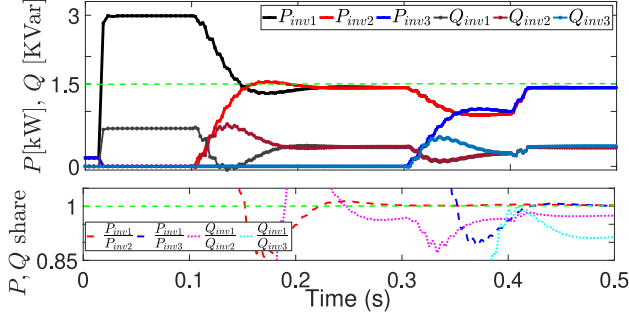
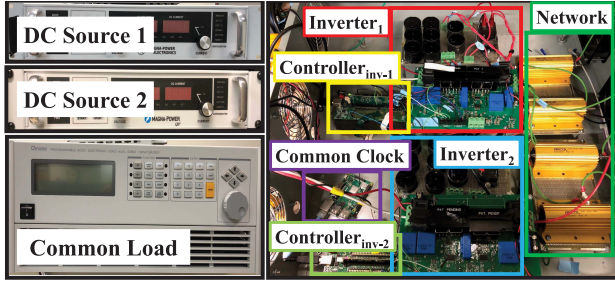
Fig. 9. P - Q sharing performance for the MMG with full droop.

Fig. 10. Experimental prototype for 1.2 kVA two inverter setup with common clock and network resistances.

values due to mismatch in commanded and actual reactive power (see Fig. 9). Meanwhile, the isochronous architecture provides improved transient and steady state performance during black starts, plug-and-play of VSIs and load changes even in mismatched conditions. High power sharing accuracy during plug-and-play and fast transient response demonstrates the superiority of the proposed architecture over full droop methods in MMGs.

B. Experimental Validation (Two VSI System)

Experiments are carried out in a laboratory setup as shown in Fig. 10. The experimental configuration consists of two single-phase insulated-gate bipolar transistor-based H-bridge inverter units along with LC output filter and controller unit for each, a purely resistive network, a variable common load served by both inverter units, and a Raspberry Pi-based (RPI) clock pulse generator. The RPI unit provides clock pulses with precise time-stamping. Each inverter consists of a digital input module to emulate a GPS receiver. All inverters synchronize

TABLE III
PARAMETERS FOR EXPERIMENTAL PROTOTYPE

Parameters	Values
Cut off frequency (ω_p)	1 (Hz)
Nominal Voltage/Frequency at PCC	120 V/60 Hz
Branch Resistance	0.2 Ω
Inverter DC Link Voltage	250 V
Inverter Filter Inductance	0.063 mH
Inverter Filter Capacitance	1 μF
Rated Power of Inverters	0.6 kVA

their local clocks, using zero-crossing detection and pulse counting, to the RPI clock signal transmitted as a square wave. This clock signal is then used to generate sinusoidal references to individual inner-loop controllers. Each inverter unit is rated as 0.6 kVA operating and utilizing a switching frequency of 20 kHz. The active power control including active power calculation and droop control, reference voltage generation, inner voltage and current controller, and PWM generation, digital input module are implemented on a TMS320F28335 digital signal processor. The inverter and network parameters are provided in Table III. The value of the droop coefficients for both inverters, — i.e., n_1, n_2 are selected as 2×10^{-4} V/W. The loop-shaping controllers K_{curk} and K_{volk} are designed as described in Section II-A with bandwidths 980 Hz and 600 Hz, respectively, for closely tracking sinusoidal references.

To verify the proposed VP-D control of the multi-inverter system, two case studies are conducted for experimental validation of the active and reactive power sharing performance (as shown in Fig. 11) using the hardware prototype. Case 1 considers two inverters serving a common load of $S_{tot} = 0.87$ kVA with transition at $t = 2.22$ s to $S_{tot} = 0.61$ kVA maintaining unity power factor throughout. Meanwhile, Case 2 studies two inverters serving a common load of $S_{tot} = 0.6$ kVA with transition at $t = 2.34$ s to $S_{tot} = 0.84$ kVA maintaining 0.8 power factor throughout.

In Case 1, both inverters are assigned with asymmetric active power references of $P_{inv1}^* = 0.56$ kW and $P_{inv2}^* = 0.31$ kW throughout the operation. The active power sharing ratio of $1.8 \pm 10\%$ is maintained throughout the operation, as shown in Fig. 11(a). Moreover, the output reactive powers of both the inverters are zero, which is a direct validation of Corollary 1. The transient time of the inverter, which here is defined as the 90% settling time of the inverter's output current peak after a load step, is about 0.037 s (i.e., 2.2 cycles of 60 Hz). This demonstrates the ability of the proposed controller to inject real power into the network to provide ancillary support to the microgrid in fast- (primary response) timescale regimes. Fig. 11(c) shows the voltage and output current waveforms of both inverters before and after the load transition. There is a finite active power mismatch ($\Delta \approx +4.44\%$) that causes a deviation ($\approx +2.5\%$) of voltage magnitude at the PCC from its nominal value. These deviations are attributed to measurement error in active power at relatively low power operating conditions. Fig. 11(e) illustrates the circulating current between two inverters throughout the operation [41]. Clearly, the magnitude of the circulating current is significantly less than the nominal output current ratings

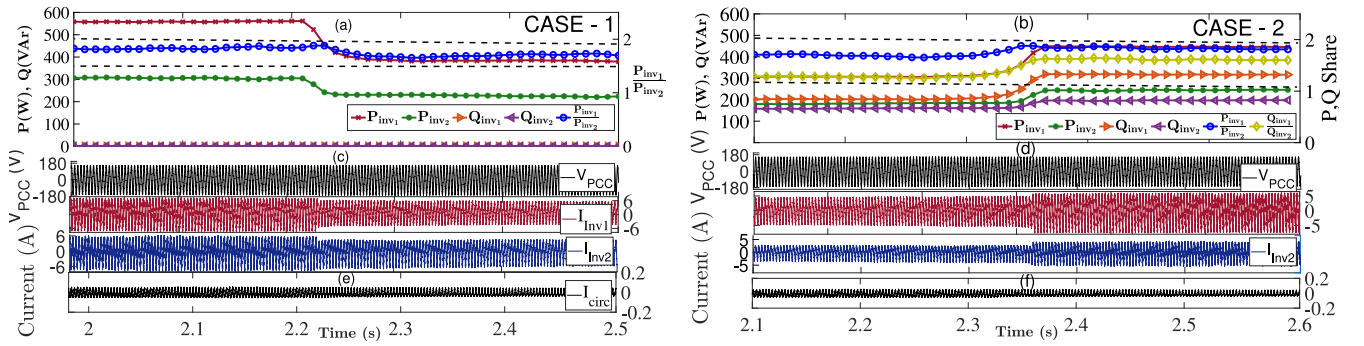


Fig. 11. Hardware results of (a) P - Q share between two parallel inverters in Case 1, (b) P - Q share in Case 2 (c) common grid voltage and output currents in Case 1, (d) common grid voltage and output currents in Case 2 and (e) circulating current in Case 1, (f) circulating current in Case 2. Case 1 has a load of 0.87 kVA with transition at $t = 2.22$ s to 0.61 kVA with $p.f. = 1.0$ and Case 2 has a load of 0.6 kVA with transition at $t = 2.34$ s to 0.84 kVA with $p.f. = 0.8$.

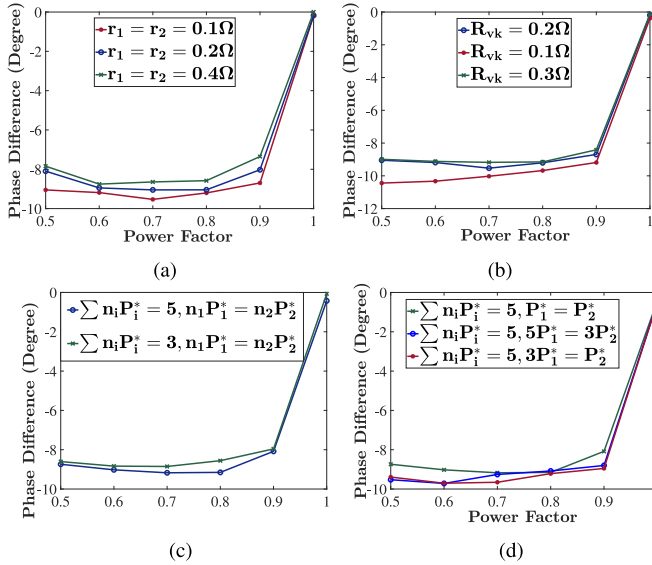


Fig. 12. Experimental results of phase difference between output currents of two inverters serving common load with varied power factors in the scenario of having various values of (a) $\sum n_i P_i^*$ with $n_1 P_1^* = n_2 P_2^*$, (b) $\sum n_i P_i^*$ with $n_1 P_1^* \neq n_2 P_2^*$.

of the inverters. The total harmonic distortion (THD) values of the voltage waveform at the PCC before and after the transition are 1.86% and 1.47%. These values are also maintained within acceptable standards [42]. Similarly, in Case 2, the inverters are assigned asymmetric active power references of $P_{inv1}^* = 0.3$ kW and $P_{inv2}^* = 0.18$ kW throughout the operation. The sharing ratio of active power is maintained at 1.67 throughout the operation. Moreover, reactive power is shared with a ratio of $1.2 \pm 10\%$ without implementing any dedicated Q control strategies throughout the operation. Fig. 11(d) illustrates the voltage and output current waveforms of both inverters before and after the load transition. The transient time of inverter current is 0.05 s (i.e., 2.99 cycles of 60 Hz). Here, $\Delta \approx -5.56\%$ that results in a deviation ($\approx -3\%$) in PCC voltage magnitude from its nominal. Fig. 11(f) illustrates the circulating current between the two inverters.

C. Design Considerations for the Multi-Inverter System

This section provides design guidelines to restrict limits on reactive power flows for implementing VP-D control in a multi-inverter system.

Fig. 12 shows experimental results for the variation in phase difference (inverter currents) when an electronic load (common load in Fig. 10), Z_L with apparent Power $S = 0.6$ kVA is varied in power factor from $p.f. = 0.5$ to unity. It is important to emphasize here that even with such a low power factor of the load to be served and no explicit control over reactive power flows of the system, the phase difference between currents is kept small ($\approx 10^\circ$ or less) by the proposed controller architecture.

Fig. 12(a) and Fig. 12(b) show that higher values of branch resistance and virtual resistance lead to smaller phase differences. This, however, may lead to a decrease in the accuracy of active power sharing in the network. From Fig. 12(c) and Fig. 12(d) it can be observed that a choice of smaller $\sum_i n_i P_i^*$ results in a smaller phase difference. These observations serve as design considerations to limit reactive power flows and implement an isochronous VP-D architecture in an LV multi-inverter system.

D. Controller-Hardware-in-the-Loop: Experimental Validation on Modified CIGRE Distribution Network

In order to further validate the performance of the proposed isochronous-based VP-D architecture and the viability of realizing these controllers on real-world low-cost micro-controller boards, we discuss here the experimental results of CHIL validation studies on an OPAL-RT real-time simulator (RTS). The distribution network is chosen from North American low voltage distribution feeder model (240 V_{rms} , $1 - \phi$, 60 Hz) from CIGRE Task Force C6.04.02 [43] (CIGRE Study committee C6) is modelled inside the OPAL-RT RTS using eMegaSim at 50 μs time-steps. The CIGRE model is modified to include four VSIs on Bus 1 and scaling of the loads. This modification is done to corroborate the system study of VSIs connected at a PCC (in this case Bus 1) while being connected to other DERs over a distribution network as shown in Fig. 13. VP-D controllers for VSI-1 and 2 are implemented on TI microprocessor boards receiving clock pulses from a pulse generator (1 clock pulse per 60 Hz). PWM duty as control signals are provided by the TI DSPs and provided to OPAL-RT RTS through digital input modules to drive the average inverter models inside OPAL-RT RTS. Analog output signals (output current, capacitor voltage and inductor current) are measured and provided to TI -DSPs of corresponding VSIs via ADC inputs to close the

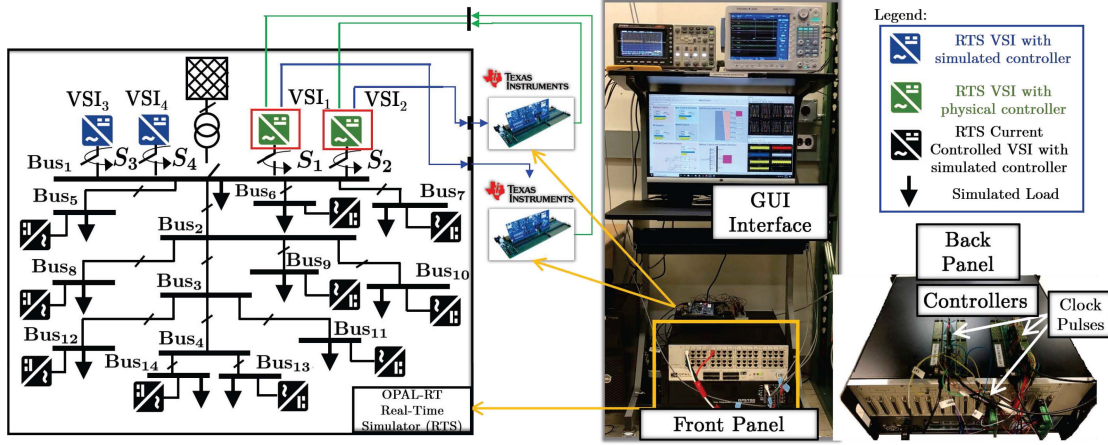


Fig. 13. Controller-Hardware-in-the-loop setup in OPAL-RT RTS with CIGRE test distribution feeder model and Texas Instruments based Delfino TMS320F28379D controllers. VSI-1, VSI-2, VSI-3 and VSI-4 receive the clock pulses and operate in VP-D control whereas other inverters operate in current controller mode interfaced with PV as DERs.

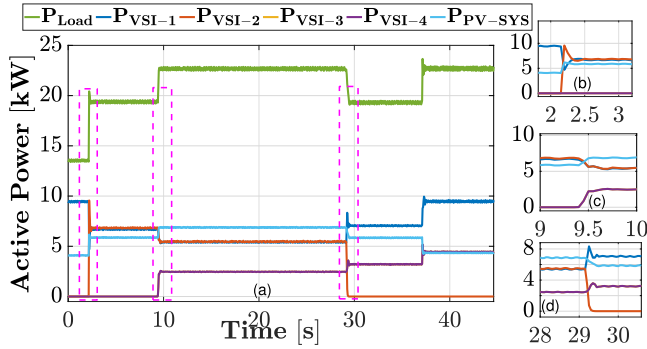


Fig. 14. (a) Active Power for CHIL experiment Case 3, (b) transition 1 at $t = 2.15$ s (c) transition 2 at $t = 9.4$ s (d) transition 3 at $t = 29.15$ s.

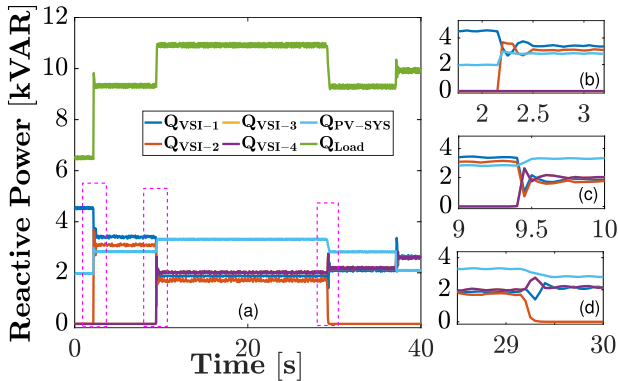


Fig. 15. (a) Reactive Power for CHIL experiment Case 3, (b) transition 1 at $t = 2.15$ s (c) transition 2 at $t = 9.4$ s (d) transition 3 at $t = 29.15$ s.

feedback loop (Fig. 13). Delay blocks are simulated inside TI DSP controllers to emulate delays in GPS clock pulses. The CHIL parameter details are shown in Table IV.

Scenario Case 3 for CHIL validation: The microgrid scenario case 3 tested in CHIL is described in Table V. Initially, VSI-1 is on and PV interfaced current controlled VSIs are operating to meet a load of 13.6 kW/6.5 kVAR. VSI-1 is maintaining the voltage and implements a multi-loop VP-D controller as described in Section II. At $t = 2.15$ s,

TABLE IV
PARAMETERS FOR CHIL SETUP

Bus No.	Source Control Mode	Load $P + jQ$ kW/kVAR	Device
1	Voltage Source Inverters VSI-1 - VSI-4	$2.5 + j 1.5$	VSI-1, VSI-2 : TI DSP (Cap. 12 kVA) VSI-3, VSI-4: Emulated in RTS (Cap. 6 kVA)
2-13	Current Controllerd VSI	$20.0 + j 9.5$	Emulated in RTS (Cap. < 2 kVA each)
14	Current Controlled VSI	$3.0 + j 0.5$	Emulated in RTS (Cap. 6 kVA)

VSI-2 is turned on and connected to the distribution feeder (demonstrating plug and play). VSI-1 and VSI-2 are prescribed $P_1^* = P_2^* = 7.1$ kW each and Bus-1 load is turned on. At $t = 9.4$ s, VSI-3 and VSI-4 are turned on and the load is increased to 22.5 kW/11 kVAR. The active power reference commands are prescribed as $P_1^* = P_2^* = 5.5$ kW and $P_3^* = P_4^* = 2.5$ kW. At $t = 29.15$ s, VSI-2 is disconnected from the network due to loss of GPS signal (described in Section IV-E later). Following the disconnection of VSI-2, Bus-1 load is disconnected in order to avoid large drooping in voltage, VSI-1, VSI-3 and VSI-4 along with feeder current controlled VSIs share the remaining load in the prescribed ratio. Note that P_1^* , P_3^* and P_4^* remain unchanged in this period as VSI-2 disconnection is an unscheduled event. Finally at $t = 57$ s, the load on Bus 14 is turned on and each VSI increases its active power in order to maintain its proportional sharing of load demand. The active power output of the network along with transients at transition events are shown in Fig. 14. Fig. 15 shows the CHIL results for reactive power outputs of inverters for case 3. Note that even though there is no explicit control of output reactive power, the proposed architecture allows equal sharing of reactive power from participating VSIs. Reactive power transients are shown to further demonstrate the performance of the VP-D architecture during load transitions. Fig. 16 summarizes the sharing ratio

TABLE V
SCENARIO CASE 3 FOR CHIL EXPERIMENTS

time (in seconds)	event details	Total Load kW/kVAR	Active Power sharing ratio
t = 0	VSI-1 ON	13.6 / 6.5	-
t = 2.15	VSI-2 ON	20/9.5	P1/P2 = 1:1
t = 9.4	VSI-3 ON Load at Bus 1 ON	22.5/11.0	P3/P4 = 1:1 P1/P3 = 2.2:1
t = 29.15	VSI-2 OFF Load at Bus 1 OFF	20.0/9.5	P3/P4 = 1:1 P1/P3 = 2.2:1
t = 57	Load at Bus 14 ON	23.0/10	Same as above

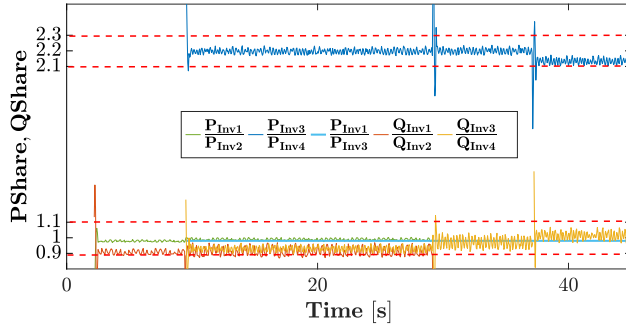


Fig. 16. Active (P), reactive (Q) power sharing ratio among VSIs for CHIL experiments of Case 3.

of active and reactive power among various VSIs. It can be clearly observed that prescribed sharing ratios are maintained well within $\pm 10\%$ even during disconnection of VSI-2 and during various load transitions. Finally, Fig. 17 shows the circulating currents among participating VSIs, as they become available, measured based on the VSI line currents and in accordance with the sharing ratios provided. Circulating currents are observed to be < 2 A (5% of rated output current) throughout for all the VSI pairs. Output voltages of each VSI are verified to be within $\pm 10\%$ throughout.

E. Effect of Delay on Active Power, Reactive Power and Circulating Currents

This section studies the effect of delays in receiving GPS clock timing pulses by a VSI in the network. Furthermore, a mitigation mechanism is provided whereby each VSI locally monitors the delay in receiving the timing pulses from the GPS based on a local clock and can disconnect from the rest of the MMG based on a user-defined delay tolerance. GPS clock pulses are provided to VSI-1 and VSI-2 via digital inputs of the TI DSP boards. Delay blocks are implemented inside TI DSP controllers, running at a time step, $T_s = 100 \mu s$, to emulate delays in GPS clock pulses. In order to characterize the effect of delay, the CHIL setup of Fig. 13 is chosen with only VSI-1 and VSI-2 connected to a load (5.7 kW/ 2.8 kVA) on Bus 1. In this setup, VSI-1 receives GPS clock pulses at no delay whereas the delay in receiving GPS signals by VSI-2 is increased subsequently and its effect on active, reactive power and circulating currents are observed. The results are shown in

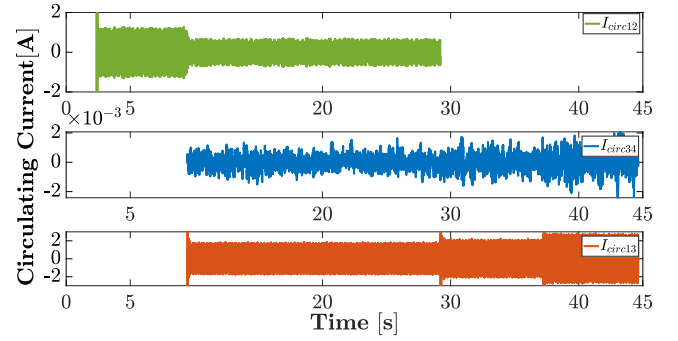


Fig. 17. Circulating Current VSI-1 and VSI-2 (top); VSI-3 and VSI-4 (middle) and VSI-1 and VSI-3 (bottom) for CHIL experiments of Case 3.

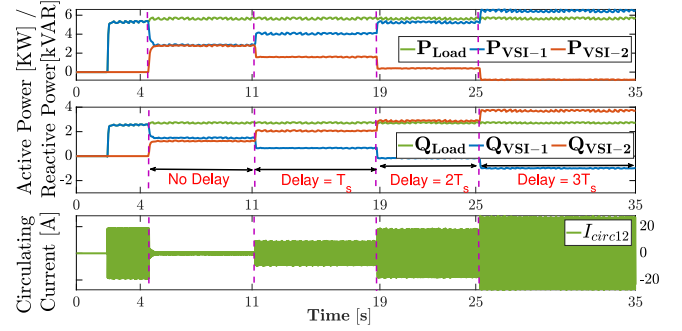


Fig. 18. CHIL simulations for characterizing the effect of delay in clock pulses on active power, reactive power and circulating current with $T_s = 1 \times 10^{-4}$ s.

Fig. 18. At $t = 2$ s, VSI-1 is turned on to serve load at Bus-1. At $t = 4.4$ s, VSI-2 is turned on and $P_1^* = P_2^* = 2.85$ kW for symmetric sharing. At $4.4 \text{ s} \leq t < 11$ s, there is no delay in receiving GPS clock pulses, as a result active power sharing ratio is maintained as prescribed, reactive power sharing is close to unity and circulating current is less than 1 A. However, at $t = 11$ s, VSI-2 suffers from a delay of $T_s = 100 \mu s$ in receiving GPS clock pulses. This results in accuracy in P and Q sharing. Furthermore, the circulating current increases to ~ 6 A and the MMG operates at a degraded condition. Subsequently at $t = 18.8$ s and $t = 25.3$ s, delay is further increased to $2T_s$ and $3T_s$ respectively. Inaccuracy in P and Q sharing further increases to a point where VSI-1 starts absorbing reactive power and provides all the active power demand. Thus, for delays greater than $2T_s$, the MMG exhibits severe degradation in performance and can not be operated. It is worth noting that for delays $< 2T_s$, although the MMG has degraded performance, it remains stable demonstrating robustness of the proposed architecture towards certain delays in GPS signals experienced by the VSIs.

Remark 8: Note that a delay of $T_s = 100 \mu s$, $2T_s$ and $3T_s$ corresponds to phase differences of 2.16° , 4.32° and 6.48° respectively. The CHIL validation agrees with the eigenvalue analysis presented earlier where phase difference w.r.t. reference frame, $\theta_k \geq \pm 5^\circ$ results in the poles of the MMG being closer to the imaginary axis resulting in critical stability of the system (see Remark 7).

In order to mitigate the issues caused due to delays in receiving GPS signals, we next propose a VSI isolation mechanism.

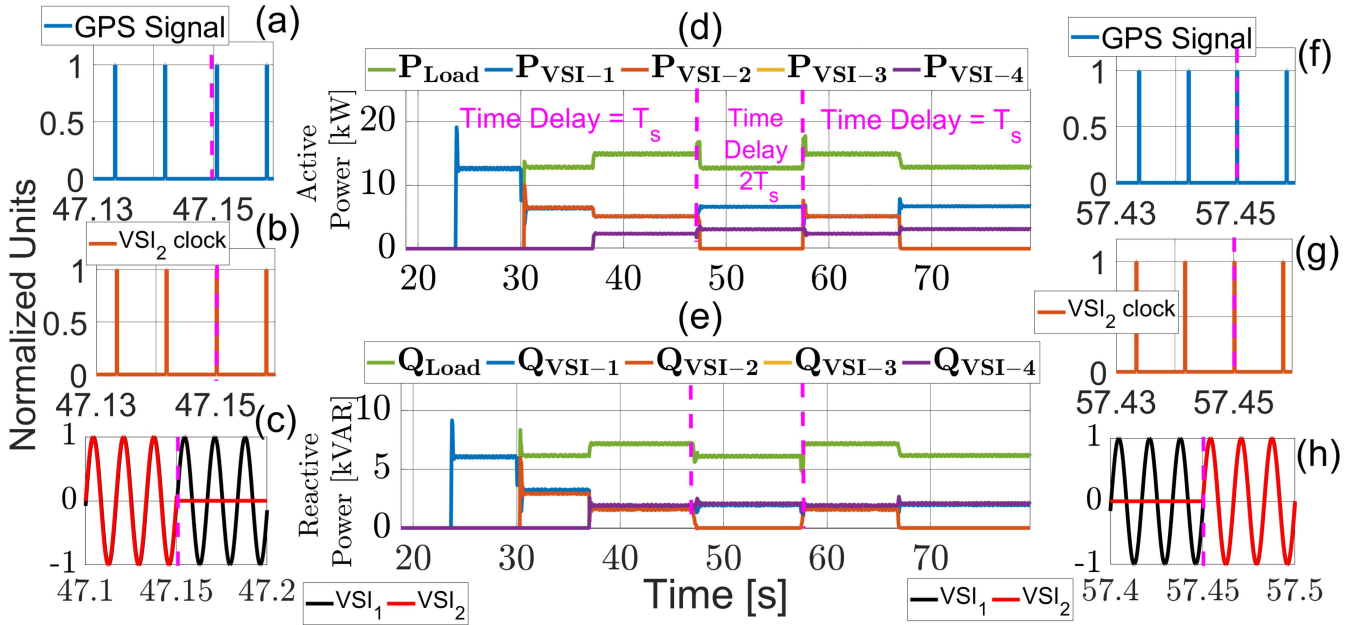


Fig. 19. Controller-Hardware-in-the-loop experiment for demonstrating VSI isolation mechanism following a communication delay in receiving the GPS signal by VSI-2. (a), (f) GPS signal received by VSI-2, (b), (g) VSI-2 local clock pulses, (c), (h) VSI-1 and VSI-2 normalized output voltage, (d) Active power output of VSIs with VSI load only, (e) Reactive power output of VSIs with VSI load only.

F. VSI Isolation Mechanism

In order to propose a VSI isolation mechanism, the following assumptions are imposed on the system.

Assumption 2: VSI local clocks are synchronized to GPS timing signals before being connected to the MMG.

Assumption 3: GPS timing signals do not arrive before they are due. That is, in case of communication delays, GPS clock pulses always lag local clock pulses.

Note that these assumptions are realistic in nature. For example, a VSI is not allowed to connect to the MMG if its local clock signals are not synchronized with GPS timing signals. In such a case, the VSI's local clock can wait for next GPS clock pulse and align with it using the GPS signal's rising edge while only incurring a delay of 1 cycle (for a GPS with 1 pulse every 60 Hz). For Assumption 3, the proposed mechanism can be easily modified to detect GPS signals in a window of time leads and lags and, if the GPS signal arrives before or after the window, the VSI can disconnect from the MMG to avoid large circulating currents.

The proposed VSI isolation mechanism is shown in Fig. 20. A delay block is used to implement delays in receiving GPS clock signals by the VSI. Following Assumptions 2 and 3, a local clock is passed through a delay tolerance block with a user-specified delay, τ_D . This block delays the local clock pulses with respect to the delayed GPS signal which are then compared using a comparator block. The comparator block generates a flag that is used as an input to a set/reset block. The output of the set/reset block is held at 'logic 0' if the delay in the GPS timing signal is less than the specified delay tolerance ($Flag = 0$) otherwise held at 'logic 1' ($Flag = 1$). The invert flag gate inverts the output bit of set/reset to generate or set the reference generation signal to zero and to close or open the VSI breaker to MMG. Finally, the external reset signal is

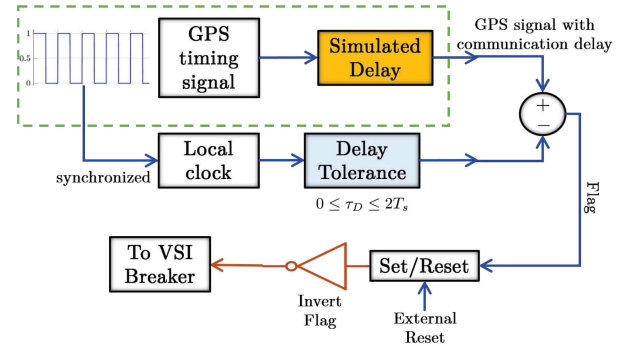


Fig. 20. VSI isolation mechanism to locally detect delays in GPS clock signals w.r.t. to a user-specified tolerance in local clock pulse to isolate or reconnect VSI to MMG.

used to reset the set/reset block while re-synchronization to the MMG is done. Note that because of Assumption 3, the flag will only be set to 1 if GPS delay $\geq \tau_D$.

The VSI isolation mechanism is validated on the CHIL setup of Fig. 13. Note that measurements pertaining to current controlled VSIs are not shown here for simplicity. A scenario similar to Case 3 is followed. However, VSI-2 is chosen to have communication delays in receiving the GPS clock signals. For $30 \text{ s} \leq t \leq 47.15 \text{ s}$, the delay is set to be $T_s = 100 \mu\text{s}$, for $47.15 \text{ s} \leq t \leq 57.45 \text{ s}$ delay of $2T_s$ and for $t > 57.45 \text{ s}$ delay of T_s is set. A delay tolerance of $\tau_D = T_s$ is chosen for VSI-2 local clock. The complete results of the CHIL experiment are shown in Fig. 19.

At $t = 47.15 \text{ s}$, the delay in receiving the GPS signal by VSI-2 increases from T_s to $2T_s$ (Fig. 19(a), (b)) as a result of which the VSI isolation mechanism sets VSI-2 breaker to off. VSI-2 output reference and hence, its output voltage, active, reactive power reduces to zero (Fig. 19(c), (d), (e)).

VSI-1, VSI-3 and VSI-4 compensate for the disconnection of VSI-2 and the output active and reactive power is maintained along with the desired sharing ratios. Note that VSI-2 keeps receiving GPS clock pulses while being disconnected from the MMG. At $t = 57.45$ s, the delay between VSI-2's local clock and the GPS clock pulses reduces to T_s (Fig. 19(f), (g)). As a result, VSI-2 reference voltage generation begins (Fig. 19(h)) and the VSI-2 breaker to MMG is switched On. This is further evident from the active and reactive power output of VSI-2 following re-connection at $t = 57.45$ s. This validates the performance of the VSI isolation mechanism in the proposed isochronous VP-D architecture.

Remark 9: Fig. 19 also demonstrates the 'plug-and-play' of the VSIs in the isochronous VP-D MMG as the controller of VSI-2 was never turned off, only the reference generation and VSI breaker were turned off following the detection of a delay (greater than tolerance) in receiving GPS signal. Once the delay was detected to be within tolerance limit, the reference generation signal started which by the virtue of the isochronous architecture is already synchronized to the MMG allowing the VSI breaker to be reconnected immediately.

V. CONCLUSION

In this article, a voltage-active power half-droop was proposed and demonstrated to show high power sharing accuracy during VSI plug-and-play and fast transient response of the proposed architecture over full-droop methods in a resistive LV ac microgrid. A loop shaping-based control law was designed for a single inverter unit to enable close regulation of the reference sinusoidal voltage signal to be tracked. A novel isochronous architecture was also proposed to maintain the system frequency and facilitate plug and play, active power sharing between VSIs in the multi-inverter system. The main advantage of the proposed architecture is to keep the reactive power flows small among the inverters without implementing an explicit $Q-f$ droop law, thereby, reducing the overall complexity of the inverter controllers. Small signal based stability analysis was conducted to show the feasibility of the proposed architecture for various scenarios of the MMG system. Moreover, analytical results were derived to provide design guidelines for selecting droop gains when there are active power mismatches and uncertainties in the load present in the LV microgrid. A VSI isolation mechanism has also been proposed to detect locally delays in GPS signals (with respect to a tolerance value) and the ability to disconnect from the MMG. Experimental and CHIL results were provided for various scenarios that validate the performance and capabilities of the proposed controller architecture.

APPENDIX

Proof of Theorem 1:

The steady-state tracking error is:

$$\begin{aligned} \lim_{s \rightarrow 0} s \left[[V_{refk}(s) - R_{vk}I_k(s)] - [G_k V_{refk}(s) - Z_k I_k(s)] \right] \\ = \lim_{s \rightarrow 0} s(1 - G_k)V_{refk}(s) - \lim_{s \rightarrow 0} s(R_{vk} - Z_k)I_k(s) \end{aligned}$$

Suppose K_{volk} has poles at $\pm j\omega_0$. Hence, using Internal Model Principle and the final value theorem, it follows that

$\lim_{s \rightarrow 0} s(1 - G_k) \frac{\omega_0}{s^2 + \omega_0^2} = 0$. Similarly we can rewrite $Z_k = G_k R_{vk} + (1 - G_k) \left(\frac{1}{sC_k} \right) \frac{1}{1 + G_{ck}K_{curk}}$. This implies $\lim_{s \rightarrow 0} s(R_{vk} - Z_k) \frac{\omega_0}{s^2 + \omega_0^2} = 0$.

Proof of Theorem 2: For clarification, $\mathbf{R}_v := \text{diag}(R_{v1}R_{v2} \dots R_{vN})$. Also, $\mathbf{V}_{ref}$ can be written as $\mathbf{E}\mu(s)$, where $\mu(s) = \frac{\omega_0}{s^2 + \omega_0^2}$ is the Laplace transform of a sinusoid with frequency ω_0 . Using the Woodbury matrix identity and matrix manipulation:

$$\begin{aligned} \mathbf{Y}(s)^{-1} &= \mathbf{\Lambda}^{-1} + \eta \mathbf{1}\mathbf{1}^T, \quad \eta := h(s)1 - h(s)\mathbf{\lambda}^T \mathbf{\Lambda}^{-1} \mathbf{\lambda}^{-1} \\ \text{Therefore, } \mathbf{I}(s) &= \left(\mathbf{Y}(s)^{-1} + \mathbf{R}_v \mathbf{I} \right)^{-1} \mathbf{E}\mu(s) \\ &= \left(\underbrace{(\mathbf{\Lambda}^{-1} + \mathbf{R}_v \mathbf{I})}_{\mathbf{\Lambda}_v^{-1}} + \eta \mathbf{1}\mathbf{1}^T \right)^{-1} \mathbf{E}\mu(s) \\ &= \left[\mathbf{\Lambda}_v - \eta \frac{\mathbf{\Lambda}_v \mathbf{1}\mathbf{1}^T \mathbf{\Lambda}_v}{1 + \eta \mathbf{1}^T \mathbf{\Lambda}_v \mathbf{1}} \right] \mathbf{E}\mu(s) \\ &= \mathbf{\Lambda}_v \mathbf{E}\mu(s) - \alpha \mathbf{\lambda}_v \mathbf{\lambda}_v^T \mathbf{E}\mu \\ \text{where } \alpha^{-1} &= Z_L^{-1} + \sum_m (r_m + R_{vm})^{-1} \\ \mathbf{\lambda}_v &= \left(\frac{1}{r_1 + R_{v1}} \quad \dots \quad \frac{1}{r_N + R_{vN}} \right)^T \\ \mathbf{\Lambda}_v &= \text{diag} \left(\frac{1}{r_1 + R_{v1}}, \dots, \frac{1}{r_N + R_{vN}} \right) \end{aligned}$$

Thus, it follows that for the k^{th} inverter in the steady state:

$$i_k(t) = I_k \sin(\omega_0 t + \phi_k)$$

where:

$$\begin{aligned} I_k &= \left(\sum_{m=1}^N \frac{E_m}{r_m + R_{vm}} \right) \frac{\gamma_k}{r_k + R_{vk}} \\ \gamma_k &= \sqrt{(\beta_k - |\alpha| \cos \angle \alpha)^2 + |\alpha|^2 \sin^2 \angle \alpha} \\ \beta_k &= E_k \left(\sum_{m=1}^N E_m (r_m + R_{vm})^{-1} \right)^{-1} \\ \cos \phi_k &= (\beta_k - |\alpha(j\omega_0)| \cos \angle \alpha(j\omega_0)) / \gamma_k; \\ \sin \phi_k &= (-|\alpha(j\omega_0)| \sin \angle \alpha(j\omega_0)) / \gamma_k; \end{aligned}$$

By denoting $|\alpha| = |\alpha(j\omega_0)|$ and $\angle \alpha = \angle \alpha(j\omega_0)$,

$$\tan \phi_k = \frac{-|\alpha| \sin \angle \alpha}{\beta_k - |\alpha| \cos \angle \alpha(j\omega_0)} = \frac{\sin \angle \alpha}{\cos \angle \alpha - \frac{\beta_k}{|\alpha|}}$$

Now, from Theorem 1:

$$\begin{aligned} v_k(t) &= V_{refk}(t) - R_{vk}i_k(t) = E_k \sin(\omega_0 t + \psi_k) \\ \text{where } V_k &= \sqrt{(E_k - R_{vk}I_k \cos \phi_k)^2 + (R_{vk}I_k \sin \phi_k)^2} \\ \text{and } \tan \psi_k &= \frac{-R_{vk}I_k \sin \phi_k}{E_k - R_{vk}I_k \cos \phi_k} = \frac{\sin \phi_k}{\cos \phi_k - \frac{E_k}{R_{vk}I_k}}. \end{aligned}$$

Proof of Theorem 3: From the expression of $\tan \phi_k$ deduced

in the previous proof. Now, $\tan(\phi_k - \phi_j)$:

$$\begin{aligned}
 &= \frac{\sin \angle \alpha}{\cos \angle \alpha - \beta_k/|\alpha|} - \frac{\sin \angle \alpha}{\cos \angle \alpha - \beta_j/|\alpha|} \\
 &= \frac{1 + \prod_{l=k,j} \left(\frac{\sin \angle \alpha}{\cos \angle \alpha - \beta_l/|\alpha|} \right)}{\left((\beta_k - \beta_j)/|\alpha| \right) \sin \angle \alpha} \\
 &= \frac{\prod_{l=k,j} (\cos \angle \alpha - \beta_l/|\alpha|) + \sin^2 \angle \alpha}{(\delta_k - \delta_j) \sin \angle \alpha / (|\alpha| \lambda_v^T (\mathbf{1} + \delta))} \\
 &= \frac{\prod_{l=k,j} (\cos \angle \alpha - \beta_l/|\alpha|) + \sin^2 \angle \alpha}{(\delta_k - \delta_j) \sin \angle v / (|v| (1 + \xi^T \delta))} \\
 &= \frac{\prod_{l=k,j} \left(\cos \angle v - \frac{1 + \delta_l}{(1 + \xi^T \delta) |v|} \right) + \sin^2 \angle v}{\frac{\text{Im}(v)(\delta_k - \delta_j) / (1 + \xi^T \delta)}{\prod_{l=k,j} \left(\text{Re}(v) - \frac{1 + \delta_l}{1 + \xi^T \delta} \right) + \text{Im}^2(v)}}
 \end{aligned}$$

where $\beta_k = E_k/\lambda_v^T E = E^*(1 + \delta_k)/\lambda_v^T (1 + \delta) E^*$, $\xi = \lambda_v/\lambda_v^T \mathbf{1}$, $v := \alpha \lambda_v^T \mathbf{1}$. Note that:

$$\begin{aligned}
 \text{Im}(v) &= \text{Im}(v - 1) \approx -\text{Im}(1/Z_L \lambda_v^T \mathbf{1}) \\
 1 - \text{Re}(v) &= \text{Re}(1/Z_L \lambda_v^T \mathbf{1})
 \end{aligned}$$

Here, it is assumed that $|Z_L \lambda_v^T \mathbf{1}| \gg 1$. Assuming that δ_k are small so that: $1 + \delta_k/(1 + \xi^T \delta) \approx 1$, it follows that

$$\begin{aligned}
 \tan(\phi_k - \phi_j) &\approx -\lambda_v^T \mathbf{1} |Z_L|^2 \text{Im}(1/Z_L) (\delta_k - \delta_j) \\
 &= (\delta_k - \delta_j) \sum_{m=1}^N |Z_L| \sin \theta_L / (r_m + R_{vm}),
 \end{aligned}$$

where $\cos \theta_L$ is the power factor of the load Z_L .

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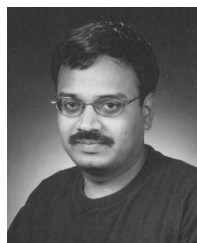
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