

Optimal Power Hardware-in-the-Loop Interfacing: Applying Modern Control For Design and Verification of High-Accuracy Interfaces

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Abstract—In this article, we develop a novel approach to designing power hardware-in-the-loop (PHIL) simulation interfaces that maximizes simulation bandwidth and accuracy by leveraging a modern control framework that explicitly considers objectives on accuracy and can automatically synthesize an optimal controller that meets these objectives while stabilizing the closed-loop system. The method developed improves upon common approaches to PHIL interface design that typically involve multiple design steps for manual compensation and stabilization that can result in interfaces that are stable but have suboptimal bandwidth and accuracy. The approach developed is general and can be applied to most PHIL system configurations. The modeling framework allows for the inclusion of scaling factors and hardware-under-test current injection models that are common to practical PHIL simulations and have significant impacts on stability. We also present practical methods and metrics for verifying the absolute accuracy of PHIL simulation results without relying on relative comparisons to potentially inaccurate models or previous simulation results. We demonstrate the accuracy evaluation method and show the improved performance achievable when using the optimal PHIL interface design approach in an experimental case study involving a 100-kVA battery inverter.

Index Terms—power hardware-in-the-loop (PHIL) simulation, accuracy, stability, h-infinity control, optimal control

I. INTRODUCTION

MODERNIZATION of electric grids worldwide continues in earnest, with increasing deployments of distributed energy resources, flexible loads, and new control infrastructure. The convergence of these new technologies inherently increases the complexity of the power system and maintaining safe, reliable, and efficient operation of modern grids relies on the successful integration of many new technologies together. Power hardware-in-the-loop (PHIL) simulation is an

important tool for derisking modern grid technologies in a controlled laboratory setting in which actual at-power devices and systems are interconnected in software simulations of complex, large-scale power system scenarios. Using PHIL, the closed-loop interaction between the hardware under test (HUT) and the simulated power system can be evaluated under a variety of grid configurations and repeatable operational scenarios without the expense or risk of a field deployment. However, for PHIL simulation results to be representative of expected real-world operations, the power interface between the simulated system and the HUT must be carefully implemented to ensure stable and accurate closed-loop simulation.

In the PHIL literature, significant attention is paid to designing solutions that focus on the stability of the PHIL simulation as stability is a necessary condition. Common approaches include augmenting the underlying interface algorithm (see [1]–[3]) used to connect the simulated model to the HUT to enhance stability by adding series inductance to the HUT [4]; moving a portion of the simulated system's impedance to the HUT [5]; adding low-pass feedback current filtering (FCF) [4], [6], [7]; including parallel high-pass filtering [8] or virtual impedance [9] at the power interface; using impedance matching [10]–[12]; or employing multirate partitioning [13]. When designing stable PHIL simulation interfaces, often the implications of a design on the PHIL simulation's accuracy are not fully considered. For example, early designs of the FCF technique (e.g., [6]) demonstrated its ability to improve stability, but results showed significant phase lag. Even a seemingly small phase lag can result in significant error between measured HUT power and the corresponding power injected in the PHIL simulation. For example, three PHIL simulation studies [14]–[16] considering active devices as HUT and applying FCF reported errors of 10%–40% in active and reactive power before further compensation. Similarly, many of the stability enhancement approaches listed above add phase lag to the closed-loop simulation, which can result in significant errors and diminish the value of such simulations. It is critical to stabilize PHIL simulations, but PHIL interfaces must be carefully designed and implemented while explicitly considering accuracy to ensure useful and valid results.

Another potential detriment to achieving accurate PHIL simulations is that many interface designs use simplified modeling assumptions such as considering an idealized power amplifier with no dynamics (e.g., [17], [18]) or neglecting the dynamics and delay of the feedback current sensor (e.g., [9], [14], [19]). Failing to model these impacts on the closed-loop system's dynamics can lead to a blunt interface design approach in

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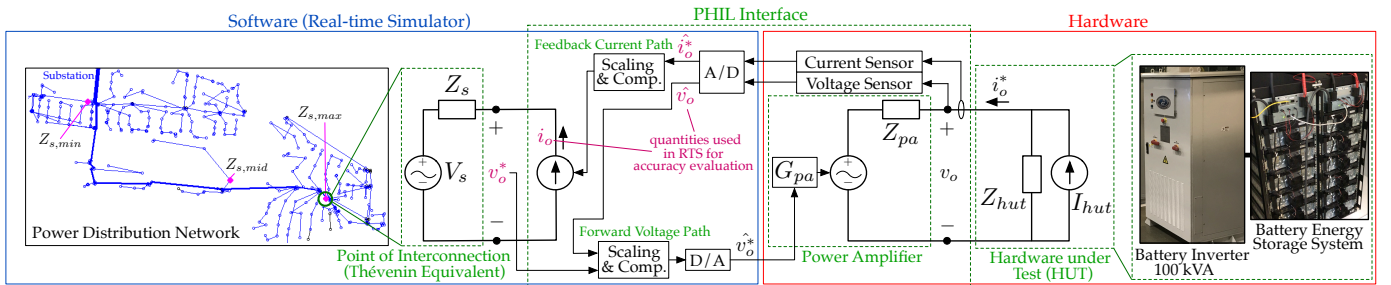


Fig. 1. PHIL simulation configuration (per phase) for an experiment evaluating a three-phase, four-quadrant, 100-kVA battery inverter system (the HUT) interconnected at various points (with source impedances $Z_{s,min}$, $Z_{s,mid}$, and $Z_{s,max}$) in a simulated electric distribution network. This configuration uses the V-ITM interface algorithm to independently interconnect each phase of a real-time simulated power distribution network (represented by a Thévenin equivalent model) with the HUT through the power interface. For the forward voltage path, the reference voltage, v_o^* , at the point of interconnection in the simulated power system model is used to provide a physical reference signal, $\hat{v}_o^*$, to the power amplifier in order to achieve output voltage, v_o , at the terminals of the HUT. A measurement of this output voltage, $\hat{v}_o$, is used as feedback to the forward voltage path compensator. The HUT responds to the voltage at its terminals and its measured current response, i_o , is measured as $\hat{i}_o$ and used as a reference for the current injection, i_o , into the simulation. Quantities v_o^* , $\hat{v}_o$, i_o and, $\hat{i}_o$ are recorded at the RTS and used for accuracy evaluation.

which stabilizing solutions are overapplied, resulting in lower bandwidth and less accurate results. For example, [15] identified instability in a PHIL experiment that occurred because of resonance between the HUT and the power amplifier's output filter at a particular frequency. In this example, stability can be achieved by applying low-pass FCF with a cutoff frequency below the resonant frequency; however, the filter will needlessly limit the bandwidth of the measured current and will add phase delay, which will also need to be compensated. Instead, by fully modeling the PHIL interface, more precise stabilization approaches that preserve simulation bandwidth and accuracy can be designed. In [15], the authors employed a manual, multi-step design process to address the specific resonance condition and compensate for the phase delay to correct the power mismatch. Instead, we propose using a systematic approach to include all interface component models and then *synthesizing* (instead of manually designing) a single, optimal controller that stabilizes the closed-loop system while maintaining optimum simulation bandwidth and accuracy.

Many PHIL interface solutions employ the widely used voltage divider circuit consisting of a simulated impedance in series with another passive impedance as the HUT (e.g., see [2], [6], [8], [11], [12], [18]–[28]) for a design case study. However, with this model, two important aspects of many practical PHIL simulations are ignored: 1) many HUT are active devices that inject (or sink) current without changing their nominally connected impedance (i.e., the feedback current is not simply a linear function of the voltage), and 2) scaling factors are often used to amplify the HUT feedback current to represent a larger device in the simulated system. Both aspects can have significant impacts on PHIL simulation stability and accuracy. In the design approach developed in this article, we leverage a more general modeling framework that explicitly incorporates active devices and scaling factors and is thus applicable to a wider range of practical PHIL configurations.

Beyond the PHIL interface design stage, rigorous accuracy validation of final PHIL simulation results is often omitted. References [4], [5], [19], [22], [28] make helpful contributions in modeling PHIL simulation accuracy; however, the common approaches they employ—including predicting accuracy only for the modeled system, but not for actual results (e.g., [19], [22]); evaluating accuracy as a comparison between PHIL

simulation and modeled results (e.g., [28]); or considering experiment accuracy only on a relative basis among multiple experiments (e.g., [4], [26])—limit their practical use in quantifying how accurate an individual PHIL simulation result is. Many of these approaches rely on an implicit assumption that models are accurate, but in many cases accurate models of the HUT and possibly other PHIL interface components are not available. Also, many studies only compare between the modeled interconnection point voltage and the voltage at the HUT's terminals (e.g., [5], [19], [22], [28]). Such evaluations do not provide a complete assessment of closed-loop system accuracy because they consider only the accuracy of the forward path from the simulated model to the power amplifier and ignore common inaccuracies in the feedback path, such as phase shift. For example, it is possible to design a voltage ideal transformer model (V-ITM) algorithm-based interface where the HUT voltage perfectly tracks the model's reference but still has feedback current with significant phase lag, resulting in power tracking error. In this article, we propose a method and metrics to evaluate closed-loop PHIL simulation accuracy that are easily applied to actual experiments, do not rely on accurate models for comparison, and give practical quantification of closed-loop performance.

We now summarize the main contributions of this work:

- 1) We develop a general approach to designing PHIL interfaces that explicitly considers objectives on accuracy and enables the synthesis of an optimal controller that stabilizes the closed-loop system while maintaining optimum simulation bandwidth and accuracy. The modeling framework includes practical scaling factors and HUT current injection models.
- 2) We present a practical method and metrics for verifying the accuracy of PHIL simulation results that are easily applied to actual experiments. The method evaluates the performance of the entire closed-loop system and uses simple metrics to quantify absolute PHIL simulation accuracy in terms that can also be used to benchmark results against other experiments.
- 3) We demonstrate the process of applying the PHIL interface design approach and verifying the accuracy of PHIL simulation results in a real-world PHIL simulation case study involving a 100-kVA battery inverter system

integrated with a simulated electric distribution system. We examine multiple system interconnection scenarios and HUT operating points to validate the performance of the designed PHIL interface.

The article is organized as follows: The optimal PHIL interface design approach is presented in Section II, followed by the accuracy evaluation method in Section III. These methods are applied in a practical case study in Section IV, and Section V concludes.

II. OPTIMAL PHIL INTERFACE DESIGN AND ANALYSIS

A. Overview

The overall approach employed here is to model the full closed-loop PHIL system and then to apply $\mathcal{H}_\infty$ optimal control theory to design a single controller that stabilizes and compensates the entire closed-loop system. The V-ITM interface algorithm with both voltage and current feedback to the controller is used. Relative to most V-ITM interfaces in the literature, this approach does require an additional voltage sensor; however, the use of both voltage and current sensors is common with other popular interface algorithms such as the damping impedance method (DIM) [11], [12] and the superior performance achieved justifies the modest cost of adding a voltage sensor, which, as will be shown, is also critical for quantifying accuracy. The V-ITM interface algorithm is used versus other interface algorithms in the literature (see [3]) as it is one of the simplest to implement and, here, the designed controller ensures stability and accuracy across a wide range of operating conditions. Reference [12] demonstrates an approach to enhance the stability of the traditional DIM by continuously measuring and matching the HUT impedance; however, the approach requires a complex signal processing method, which is sensitive to uncertainty and can be slow to compute (110 ms is established), limiting the achievable simulation timescales. In contrast, our feedback control-based approach accrues robustness where uncertainties in modeling can be tolerated and the approach can be easily applied (e.g., using a transfer function) at all simulation timescales (50 μ s is verified). Thus, even though the optimal PHIL interface is synthesized based on a fixed model of the plant, when parameters in the plant vary, it still performs well, as demonstrated in Section IV-E.

In the remainder of this section, we detail how to apply the proposed interface design approach at key steps in the process of designing and implementing a stable and accurate PHIL simulation. The reader is referred to other key references [1], [29] and the forthcoming IEEE P2004 Recommended Practice [30] for more comprehensive discussions of other important steps for successful PHIL simulation implementation.

B. System Modeling and Key Nomenclature

For effective interface design and analysis, all components of the PHIL simulation configuration shown in Fig. 1 must be modeled judiciously, keeping in view the system's closed-loop performance. Here, we model the PHIL simulation configuration in the continuous-time domain using the V-ITM interface algorithm and the transfer function block diagram shown in Fig. 2(a). The continuous-time domain is most convenient for design, initial stability analysis, and optimal controller synthesis, though the final PHIL simulation implementation

will involve a hybrid model with a discrete-time simulation coupled to a continuous-time physical system. For three-phase power system configurations, such as that presented in the case study, each phase is modeled separately using the block diagram in Fig. 2(a). The block diagram used here is based on the comprehensive PHIL experiment modeling block diagram presented in our previous work [31]. The PHIL system model is general in that 1) the HUT is represented as a current injection (modeled as a disturbance) in parallel with an impedance rather than a single passive impedance, and 2) voltage and current scaling factors between the simulated model and the physical HUT are explicitly included. These factors considerably affect the stability and accuracy of the closed-loop simulation, and must be included for comprehensive design and analysis.

In Fig. 2(a), V_s and Z_s are the voltage reference and impedance for a Thévenin equivalent circuit representing the point of interconnection in the PHIL model, γ_v is the voltage scaling factor, K_v is the compensator for the voltage path, K_{ff} is the feed-forward gain for the voltage forward path (designed in Section II-C5), G_{dac} is a transfer function representing the digital-to-analog (D/A) conversion delay, $\hat{v}_o^*$ is the output voltage physical reference signal, G_{pa} is the power amplifier's transfer function, Z_{pa} is the output impedance of the power amplifier, Y_{hut} is the output admittance of the HUT, I_{hut} is the current injection from the HUT, $H_{s,v}$ and $H_{s,i}$ are transfer functions representing the voltage and current sensors, respectively, $\hat{v}_o$ is the measured output voltage, $\hat{i}_o^*$ is the measured HUT current, H_{adc} is a transfer function representing the analog-to-digital (A/D) conversion delay, H_{fb} is a compensator for the current feedback path, and γ_i is the current scaling factor. Here, Z_{pa} is explicitly modeled as many power amplifiers (e.g., all switched-mode type) have an output filter that interacts with the HUT and causes a voltage drop/rise. $Z_{pa} = 0$ can be used for power amplifiers without such a filter. Our previous work [31] provides a guide on how to identify transfer functions for each component. We summarize the specific models and parameters used in Table IV and proceed to discuss general interface design with each element represented as labeled in Fig. 2(a).

C. PHIL Interface Design

1) *Objectives:* For a stable and accurate PHIL simulation of the configuration shown in Fig. 2(a), the following objectives should be met:

- **O1. Stability:** The closed-loop PHIL system must be internally stable.
- **O2. Forward path voltage tracking:** $v_o \rightarrow v_o^*$. The voltage at the terminals of the HUT, v_o , should track the voltage at the point of interconnection in the PHIL model (after voltage scaling), v_o^* .
- **O3. Feedback path current tracking:** $i_o \rightarrow i_o^*$. The current injected into the PHIL simulation (before current scaling), i_o , should track the measured current at the terminals of the HUT, i_o^* .

2) *Approach:* In the block diagram in Fig. 2(a), K_v and H_{fb} are the two compensators to be designed to achieve objectives O1–O3. In the modern control approach we employ,

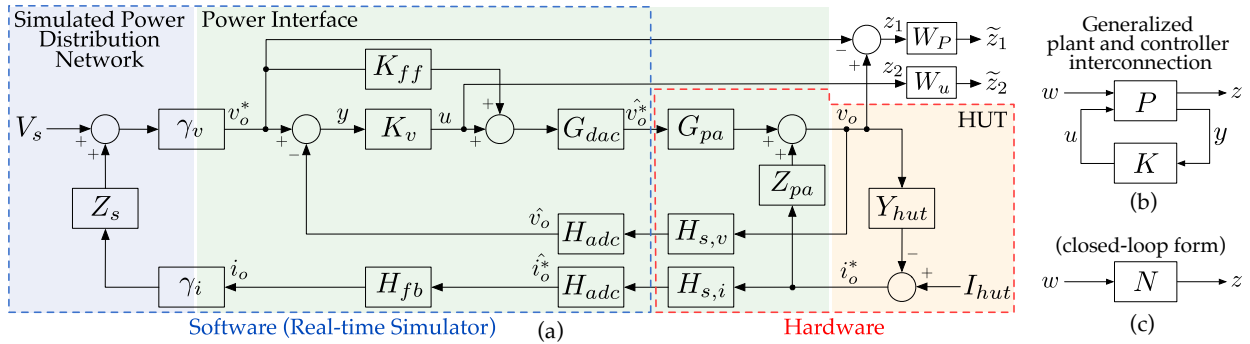


Fig. 2. Transfer function block diagram of the PHIL simulation in (a) comprehensive multiloop, (b) generalized plant and controller interconnection, and (c) generalized closed-loop forms. A listing of the individual transfer function values used for the case study is given in Table IV.

it is possible to simultaneously design both by considering them as a single multiple-input, multiple-output compensator; however, for simplicity, and because the optimal form of H_{fb} needed to achieve objective O3 can be easily identified and approximated, we fix the design of H_{fb} and then synthesize a stabilizing, optimal controller for K_v that achieves objectives O1 and O2. This two-step process maintains an optimal approach while giving the flexibility to independently design H_{fb} according to experiment-specific needs (see next section) and subsequently employing $\mathcal{H}_\infty$ optimal control theory to synthesize the more complex K_v that stabilizes and compensates the entire closed-loop system (including the dynamics of H_{fb}). Measurement $\hat{v}_o$ is given as feedback to K_v and measurement $\hat{i}_o^*$ is the input to H_{fb} .

3) H_{fb} Compensator design: Compensator H_{fb} is designed to achieve objective O3 by compensating for the delay in A/D conversion (modeled via H_{adc}) and current sensor response time and dynamics, $H_{s,i}$. It is common for current sensors used in PHIL simulations to have a bandwidth that is significantly greater than other key components (e.g., the power amplifier) in the closed-loop system. Thus, the dynamics of $H_{s,i}$ need not be explicitly compensated for; here, we focus on the delay portion of $H_{s,i}$ and the A/D conversion delay, H_{adc} . This total delay results in phase lag that increases with frequency. Some existing approaches (e.g., [14]) compensate for phase shift at the fundamental frequency, but not for the increased phase lag at higher frequencies, as is desired for high-accuracy PHIL interfaces with better dynamic performance. Dynamic phase compensation approaches based on Fourier decomposition and reconstruction [10], [32], dq0 transformation for three-phase systems [25], and the Smith predictor [33] have been introduced. For ease of analysis and control design, we consider the Smith predictor-based method which is linear and can be applied on a per-phase basis. We then introduce a transfer function fitting-based approach. Both methods, summarized in Table I, are considered to demonstrate that the $\mathcal{H}_\infty$ optimal control approach is general and we show in Section IV-E that the transfer function fitting-based approach has higher performance for the experimental case study. Before designing H_{fb} it is important to consider the requirements of the PHIL experiment; it is unrealistic to design an H_{fb} that will compensate magnitude and phase accurately at every frequency. Thus, it is recommended that the HUT first be evaluated in an open-loop mode and samples of $\hat{i}_o^*$ be analyzed to determine the HUT feedback performance range—the specific range of

harmonic frequencies present in $\hat{i}_o^*$ that must be compensated. An example of the analysis is given in Section IV.

TABLE I.
 H_{fb} DYNAMIC COMPENSATION DESIGNS CONSIDERED

Design	Implementation
Smith predictor [33]	$H_{fb,sm} = \frac{(T_{smith1/2})s}{1+T_{smith1/2}}$
Smith predictor with additional phase lead [33]	$H_{fb,smPL} = \frac{(T_{smith2/2})s}{1+T_{smith2/2}} \cdot \frac{(1+T_{smPL}s)\omega_{smHF}}{(s+\omega_{smHF})}$ (pole ω_{smHF} is added to attain roll-off at high freq.)
Transfer function fitting method	Define length N_{fb} frequency response: $\omega_{fb} = [\omega_{fb,1}, \dots, \omega_{fb,N_{fb}}]$ $\bar{H}_{fbFR} = [\bar{H}_{fbFR,1}, \dots, \bar{H}_{fbFR,N_{fb}}]$ and use transfer function estimation method such as MATLAB's <i>tfest</i> [34] to obtain an order O_{Hfb} transfer function, $H_{fb,tf}$

4) *Preparing the generalized model:* In preparation for K_v compensator design, we consolidate the multiloop, closed-loop block diagram in Fig. 2(a) into the general control configuration commonly used in modern control theory [35] shown in Fig. 2(b). Here, P is the generalized plant, K is the controller (e.g., interface compensation design), w is a vector of the exogenous inputs (e.g., commands, disturbances, and noise), z are the exogenous outputs (e.g., signals to be regulated), y are the controller inputs, and u are the control signals. Note that in this continuous-time modeling framework, all variables are functions of the Laplace variable, s , but this is not explicitly shown for notational convenience.

For the block diagram in Fig. 2(a), the exogenous inputs are $w = [V_s \ I_{hut}]^T$. The exogenous outputs are chosen to be $z = [z_1 \ z_2]^T = [(v_o - v_o^*) \ u]^T$ to emphasize a performance target of minimizing the error between v_o and v_o^* , which must be balanced against the control effort, u . Note that it is possible to include $(i_o - i_o^*)$ as a regulated variable in z ; however, it is not included here as it was seen that the performance achieved was similar with the current tracking error not explicitly included as a part of the regulated variable z in comparison to when it is included with considerably easier synthesis and implementation steps. We note that O3 is still achieved by H_{fb} . The generalized plant maps $[w \ u]^T$ to $[z \ y]^T$ as follows:

$$\begin{bmatrix} z_1 \\ z_2 \\ y \end{bmatrix} = \begin{bmatrix} v_o - v_o^* \\ u \\ y \end{bmatrix} = \begin{bmatrix} P_{11,1} & P_{11,2} & P_{12} \\ 0 & 0 & 1 \\ P_{21,1} & P_{21,2} & P_{22} \end{bmatrix} \begin{bmatrix} V_s \\ I_{hut} \\ u \end{bmatrix}$$

We solve for each component of the generalized plant. Note that v_o can be written as:

$$v_o = G_2 I_{hut} + G_3 u + G_4 V_s, \quad (1)$$

where

$$\begin{aligned} G_5 &= Z_s \gamma_i H_{fb} H_{adc} H_{s,i}, \\ G_1 &= 1 + Z_{pa} Y_{hut} + G_{pa} G_{dac} K_{ff} \gamma_v G_5 Y_{hut}, \\ G_2 &= G_1^{-1} [Z_{pa} + G_{pa} G_{dac} K_{ff} \gamma_v G_5], \\ G_3 &= G_1^{-1} G_{pa} G_{dac}, \text{ and } G_4 = G_3 K_{ff} \gamma_v. \end{aligned}$$

Next, see that v_o^* can be expressed as:

$$v_o^* = \gamma_v [V_s + G_5 (I_{hut} - Y_{hut} v_o)]. \quad (2)$$

Subtracting (2) from (1), we obtain:

$$\begin{aligned} v_o - v_o^* &= v_o - \gamma_v [V_s + G_5 (I_{hut} - Y_{hut} v_o)] \\ &= P_{11,1} V_s + P_{11,2} I_{hut} + P_{12} u \end{aligned}$$

where

$$\begin{aligned} P_{11,1} &= G_4 + \gamma_v (G_5 Y_{hut} G_4 - 1), \\ P_{11,2} &= G_2 - \gamma_v G_5 (1 - Y_{hut} G_2), \text{ and} \\ P_{12} &= (1 + \gamma_v G_5 Y_{hut}) G_3. \end{aligned}$$

Finally, note that y can be written as:

$$y = (v_o^* - H_{adc} H_{s,v} v_o). \quad (3)$$

Substituting (1) and (2) into (3), we obtain:

$$y = P_{21,1} V_s + P_{21,2} I_{hut} + P_{22} u$$

where

$$\begin{aligned} G_6 &= \gamma_v G_5 Y_{hut} + H_{adc} H_{s,v}, \quad P_{21,1} = \gamma_v - G_6 G_4, \\ P_{21,2} &= \gamma_v G_5 - G_6 G_2, \text{ and } P_{22} = -G_6 G_3. \end{aligned}$$

We can close the loop of the generalized control configuration in Fig. 2(b) to achieve the closed-loop system, N , that maps w to z , as shown in Fig. 2(c); here, $N = F_l(P, K) = P_{11} + P_{12} K (I - P_{22} K)^{-1} P_{21}$ and $F_l(P, K)$ is the lower linear fractional transformation of P with K .

5) *K_v compensator design and synthesis*: Here we describe how to design compensator K_v to achieve objectives O1 and O2. To do so, we leverage $\mathcal{H}_\infty$ optimal control, which allows us to shape the magnitude of the system's closed-loop transfer function by synthesizing a controller that minimizes user-defined $\mathcal{H}_\infty$ performance objectives. Here, $\mathcal{H}_\infty$ refers to the $\mathcal{H}_\infty$ norm, which is simply the peak value of a transfer function's magnitude as a function of frequency. That is, if $f(s)$ is a stable scalar transfer function, then its $\mathcal{H}_\infty$ norm is $\|f(s)\|_\infty := \sup_\omega |f(j\omega)|$. With the generalized model developed in Section II-C4, desired performance of the closed-loop system can be targeted by choosing frequency-dependent weights W_P and W_u in the weighted, generalized plant $\tilde{P} = \text{diag}(W_P, W_u, I)P$. This results in a weighted, generalized plant that maps w to $\tilde{z} = [\tilde{z}_1 \quad \tilde{z}_2]^T$. To achieve objective O2, we select a frequency-dependent performance weight, W_P , resulting in the variable $\tilde{z}_1 = W_P z_1 = W_P (v_o - v_o^*)$ to be regulated, allowing us to place frequency-dependent performance objectives on the closed-loop voltage tracking error transfer function.

The best selections for weights W_P and W_u are dependent on the PHIL system configuration (specific examples are given in the case study); for most PHIL simulations W_P is designed to emphasize performance at the nominal frequency, ω_0 , with high gain at that frequency and W_u is designed to limit control effort to the bandwidth of the power interface using a high-pass filter. The feedforward gain, K_{ff} , improves the overall bandwidth of the compensator's forward voltage path. A candidate K_{ff} that can be targeted is the inverse of the plant where there is no feedback (see [35]); however, the inverse may be

non-causal, unstable, and sensitive to even slight variations in the model being inverted. When used in parallel with K_v to improve voltage path compensation response time, choosing K_{ff} to be the inverse of the plant's frequency response at ω_0 (i.e., $K_{ff} = 1/|P_{22}(j\omega)|_{\omega=\omega_0}$) is a good candidate. In practice, this gain is typically lies between 0.5 and 1 and can be further adjusted iteratively (i.e., adjust K_{ff} and resynthesize K_v) as needed. Once weights are selected, the $\mathcal{H}_\infty$ optimal controller can be obtained by solving:

$$\min_{K \text{ stabilizing}} F_l(\tilde{P}, K) \quad (4)$$

This problem can be readily solved using the MATLAB Robust Control Toolbox. An algorithm for solving (4) along with the theoretical underpinnings of this optimization problem are given in [35]. Note that the solution to this problem provides a *stabilizing* K that minimizes $\tilde{N} = F_l(\tilde{P}, K)$. That is, if there is a solution, K^* , to (4), it will be a controller that stabilizes the closed-loop system; the stability of the closed-loop system is guaranteed (thus meeting objective O1) without relying on explicit manual iterations. The optimal controller K^* will have an order similar to the order of $\tilde{P}$, which may be considerable. Thus, before implementation for real-time simulation, model order reduction (e.g., see MATLAB's *balred* command) is recommended to obtain a lower order controller prior to discretization. In practice, we have found that a reduction down to the 15th order is sufficient and performs well (see Fig. 5).

D. Stability Analysis

When following the design approach outlined in Section II-C the closed-loop system is guaranteed to be stable as long as a controller can be synthesized successfully; thus, no additional stability verification of the continuous time closed-loop system model is required. The authors of [17], [23], however, suggest that it is important to also consider the effects of sampling and numerical methods inherent in the discrete time model on the stability of the final implementation. A good method to verify closed-loop stability with the discrete time model is to discretize (using the bilinear transform is recommended) K_v and H_{fb} and perform a simulation (e.g., in MATLAB Simulink) of the full hybrid system including discrete time models of all software components and continuous time models of the hardware components. See [36] for further details on simulation of hybrid systems.

III. ACCURACY EVALUATION

A. Motivation and Overview

Here, we introduce metrics for verifying the *absolute* accuracy of PHIL simulation results without relying on relative comparisons to potentially inaccurate models or previous simulation results. The framework developed in this section provides a valuable means for PHIL practitioners and researchers to easily identify the absolute accuracy of a particular simulation and compare results from two different simulations on a common basis (i.e., benchmark results). The accuracy metrics are defined solely in terms of measurements available within the PHIL simulation, thereby enabling determination of accuracy in real time during the experiment. This method

of absolute accuracy evaluation is accomplished by evaluating tracking objectives O2 and O3, which consider how well voltage and current at the HUT match voltage and current in the PHIL model, as well as how the power injected into the real-time software simulation ($S_{sw} = v_o^* i_o$) tracks the measured power at the HUT ($S_{hut} = v_o i_o$). Including metrics on voltage, current, and power allows the PHIL practitioner to pinpoint, and subsequently address, where sources of error in the PHIL simulation configuration originate. Accuracy measures using both time-domain and frequency-domain approaches are introduced to comprehensively consider tracking performance of both steady-state and instantaneous quantities across the bandwidth of the simulation.

B. Measurement Processing and Accuracy Bandwidth

As detailed in O2 and O3, the key quantities needed for accuracy evaluation are v_o^* , v_o , i_o^* , and i_o ; however, as shown in Fig. 1, v_o and i_o^* exist in the physical hardware domain while v_o^* and i_o are part of the software domain. To determine accuracy metrics based on v_o^* , v_o , i_o^* , and i_o , all quantities must be obtained in the same domain. The challenge is that A/D or D/A conversions result in a delay for conversion from one domain to the other and must be accounted for. Here, we obtain all measurements in the software domain as it enables real-time accuracy evaluation. To do so, v_o^* , $\hat{v}_o$, i_o and, $\hat{i}_o^*$ are recorded at the RTS (see Fig. 1) and then we account for the delayed phase (due primarily to A/D conversion) of $\hat{v}_o$ and $\hat{i}_o^*$ to closely approximate v_o and i_o^* . Note that we do not account for $H_{s,i}$ and $H_{s,v}$ here as they generally (and in the case study) contribute very little time delay compared to the A/D conversion and their attenuation effects within the PHIL simulation bandwidth are negligible. For ease of implementation, v_o^* and i_o (natively available in the software model) are delayed rather than advancing $\hat{v}_o$ and $\hat{i}_o^*$ (the physical domain measurements). We summarize the variables used in accuracy evaluation:

$$\begin{aligned} v_o^*(t) &= v_o^*(kT_s) = v_o^*((k-1)T_s) \\ \hat{v}_o(t) &= \hat{v}_o(kT_s) = \hat{v}_o(kT_s) \\ i_o^*(t) &= i_o^*(kT_s) = i_o^*(kT_s) \\ \hat{i}_o(t) &= \hat{i}_o(kT_s) = i_o((k-1)T_s) \end{aligned}$$

where x' denotes the transformed version of x , T_s is the real-time simulation time step, and $k \in \mathbb{N}$ is the discrete-time index. For notational convenience, we assume that the above transformations are applied prior to calculating any metrics and the $\cdot'$ notation is dropped hereafter.

The PHIL simulation's closed-loop bandwidth, BW_{SYS} , is another important factor that should be considered when calculating accuracy metrics. For example, in the case study, the HUT current (see Fig. 3) contains frequency components above the 50th harmonic (3,000 Hz); however, when BW_{SYS} is lower than the frequency of the harmonic component (e.g., BW_{SYS} is limited by the power amplifier's bandwidth of 1,950 Hz), the PHIL simulation is not expected to have accurate tracking performance at frequencies beyond BW_{SYS} and will thus not provide accuracy on a high frequency component. Therefore, for some accuracy metrics, it is useful to evaluate performance at only frequencies within BW_{SYS} , where

accurate tracking performance is expected. To do so, some accuracy metrics will use filtered quantities, $\tilde{v}_o^* = H_{sbw} v_o^*$, $\tilde{v}_o = H_{sbw} v_o$, $\tilde{i}_o^* = H_{sbw} i_o^*$, and $\tilde{i}_o = H_{sbw} i_o$. Here, we define $H_{sbw}(s)$ to be a fifth-order Butterworth filter with cutoff frequency BW_{SYS} . In the case study results (see Table V), we compare the effects of using filtered and unfiltered quantities.

Steady-state metrics are calculated using a period of $T_{ss} = 0.2s$, or 12 ac cycles at 60 Hz. This is based on the recommendations of IEEE Std. 519 [37] and strikes a balance between measurement consistency and reporting resolution.

C. Accuracy Metrics

We introduce two sets of metrics: one set (see Table II) for quantifying accuracy at the instantaneous waveform timescale and another set (see Table III) on a steady-state timescale. All metrics are demonstrated in the case study.

TABLE II.
INSTANTANEOUS WAVEFORM ERROR METRICS

Metric	Definition
Instantaneous voltage tracking error: IVTE(t)	$\frac{\tilde{v}_o(t) - \tilde{v}_o^*(t)}{\sqrt{2} \cdot \text{RMS}(\tilde{v}_o^*(t))}$
RMS instantaneous voltage tracking error: rIVTE	$\text{RMS}(\text{IVTE})$
Instantaneous current tracking error: ICTE(t)	$\frac{\tilde{i}_o(t) - \tilde{i}_o^*(t)}{\sqrt{2} \cdot \text{RMS}(\tilde{i}_o^*(t))}$
RMS instantaneous current tracking error: rICTE	$\text{RMS}(\text{ICTE})$
Instantaneous power tracking error: IPTE(t)	$\frac{\tilde{S}_{sw}(t) - \tilde{S}_{hut}(t)}{2 \cdot \text{RMS}(\tilde{S}_{hut}(t))}$
RMS instantaneous power tracking error: rIPTE	$\text{RMS}(\text{IPTE})$

The instantaneous waveform error metrics consider normalized, absolute tracking error in the instantaneous voltage, current, and power waveforms. When plotted, these metrics are well-suited for identifying performance during transient periods and for identifying sub-cycle sources of error. Calculating the root mean square (RMS) value of each metric over T_{ss} provides useful summary performance measures.

The steady-state error metrics provide a measure of accuracy performance based on quantities averaged over one or more cycles (in the case study, T_{ss} is the period used), such as active power. Active and reactive power tracking are common and important fundamental frequency-based measures of accuracy. Additional frequency-domain metrics are needed to validate the accuracy of the PHIL simulation at frequencies beyond the fundamental. We define three such metrics using Fourier components to consider current magnitude and phase tracking performance at frequencies within the HUT feedback performance range identified during the PHIL interface design stage (see Section II-C3). These metrics are based on concepts of Total Vector Error (TVE) defined in IEEE Std. C37.118 [38] and Total Harmonic Distortion (THD) as defined in IEEE Std. 519 [37]. The metric $I_{TVE,m}$ gives a percentage error characterizing how well each m^{th} harmonic frequency component of i_o^* is represented in i_o , normalized by the total amount of harmonic current present. $I_{TVE,m,n}$ provides a summary metric for how well all harmonic frequency components between the m^{th} and n^{th} harmonics are being tracked.

Note that $\theta_{sw} = \angle v_o^* - \angle i_o$ and $\theta_{hut} = \angle v_o - \angle i_o^*$ are the power factor angles for the software and measured HUT quantities, respectively; $S_{hut,nom}$ is the nominal apparent power rating of the HUT; $x_{y,m} \angle \phi_{y,m}$ denotes the RMS

magnitude and phase, calculated over period T_{ss} , of the m^{th} harmonic frequency component of quantity x_y (used as voltage or current here); $\text{THD}(x_y)$ is the per unit THD [37] of x_y calculated based on harmonic frequencies less than BW_{SYS} over period T_{ss} ; and $\|\vec{x}\|_2$ is the Euclidian norm of $\vec{x}$.

TABLE III.
STEADY-STATE ERROR METRICS

Metric	Definition
APTE	Active power tracking error: $\text{APTE} = \frac{\text{RMS}(S_{sw}) \cos \theta_{sw} - \text{RMS}(S_{hut}) \cos \theta_{hut}}{S_{hut, \text{nom}}}$
RPTE	Reactive power tracking error: $\text{RPTE} = \frac{\text{RMS}(S_{sw}) \sin \theta_{sw} - \text{RMS}(S_{hut}) \sin \theta_{hut}}{S_{hut, \text{nom}}}$
FCATE	Fundamental current angle tracking error: $\text{FCATE} = \phi_{i_o, 1} - \phi_{i_o^*, 1}$
$I_{TVE, m}$	Normalized current TVE at the single m^{th} harmonic frequency: $I_{TVE, m} = \frac{i_{o, m} \angle \phi_{i_o, m} - i_{o^*, m} \angle \phi_{i_o^*, m}}{i_{o^*, 1} \cdot \text{THD}(i_o^*)}$
$I_{TVE, m, n}$	Total normalized current TVE including the range $[m, n]$ of harmonic frequencies: $I_{TVE, m, n} = [I_{TVE, m} \quad \dots \quad I_{TVE, n}]^T$

IV. EXPERIMENT CASE STUDY

A. Experiment Configuration

The PHIL experiment configuration in Fig. 1 was used to evaluate a three-phase, 100-kVA, four-quadrant inverter with a 33-kWh Lithium-ion battery energy storage system, interconnected at various points in an electric distribution network. Each phase of the HUT was interconnected to the appropriate phase of the distribution network model using an independent version of the single-phase configuration shown in Fig. 1. The PHIL interface for this experiment consisted of 1) a three-phase (with independent phase control), 270-kVA Ametek RS-series power amplifier; 2) a set of three (one per phase, connected line-neutral) LEM DVL1000 voltage transducers for output voltage measurement; and 3) a set of three LEM LTC-600-SF current transducers for current feedback measurement. The electric distribution feeder model used is from a real-world system in Colorado, USA, and was analyzed to determine the interconnection impedance (determined via short-circuit impedance values) at multiple three-phase interconnection nodes along the length of the approximately 4-mile-long distribution feeder. An Opal RT OP5700-series real-time simulator with a time step of $T_s = 50 \mu\text{s}$ was used to execute the real-time distribution system model and three discrete-time PHIL interface compensators.

B. System Modeling

Modeling detail for each element in the closed-loop system is given in Table IV. Note that all time delays were approximated by a second-order Padé approximation because rational transfer functions are required for controller synthesis and first-order Padé approximations can lead to modeling inaccuracies [27]. The generalized plant was obtained following the process outlined in Section II-C4.

C. PHIL Interface Design

1) *Base case interfaces*: To emphasize the benefits of the optimal interface, we consider two base case interfaces for

TABLE IV.
SYSTEM MODELING ELEMENTS

Element	Value	Modeling Basis
T_s	$50 \mu\text{s}$	Real-time simulation time step
$Z_{s, \min}$	$53.3e^{-3} + s150.3e^{-6} \Omega$	Distribution feeder model, short-circuit impedance near substation
$Z_{s, \max}$	$163.4e^{-3} + s565.4e^{-6} \Omega$	Distribution feeder model, short-circuit impedance near end of three-phase trunk
γ_v	$\frac{0.480 \text{ kV}}{13.2 \text{ kV}}$	Scale modeled system nominal voltage to that of physical HUT
G_{dac}	$\frac{(T_s^2/12)s^2 - (T_s/2)s + 1}{(T_s^2/12)s^2 + (T_s/2)s + 1}$	Single time step delay for D/A conversion (as 2^{nd} order Padé approx.)
G_{pa}	$\frac{1}{(1/2\pi 1950)s + 1} e^{-s50e^{-6}}$	Delay and single pole filter model previously identified in [15]
Z_{pa}	$26e^{-3} + s53.2e^{-6} \Omega$	Physical measurement
Y_{hut}	$s \frac{2}{3} 70e^{-6} \text{ S}$	Vendor-supplied inverter wiring diagram. See [31] for model structure derivation.
$H_{s, v}$	$\frac{1}{(1/2\pi 15000)s + 1} e^{-s20e^{-6}}$	Delay and single pole filter model. Delay and bandwidth information provided on datasheet.
$H_{s, i}$	$\frac{1}{(1/2\pi 100000)s + 1} e^{-s1e^{-6}}$	Delay and single pole filter model. Delay and bandwidth information provided on datasheet.
H_{adc}	$= G_{dac}$	Single time step delay for A/D conversion
$\gamma_{i, \min}$	$\frac{(1 \text{ MVA}/13.2 \text{ kV})}{(0.1 \text{ MVA}/0.480 \text{ kV})}$	Scale 100-kVA physical inverter to represent 1-MVA inverter in simulation model
$\gamma_{i, \max}$	$\frac{(1 \text{ MVA}/13.2 \text{ kV})}{(0.1 \text{ MVA}/0.480 \text{ kV})}$	Scale 100-kVA physical inverter to represent 5.5-MVA inverter in simulation model

comparison. The first, denoted “CVI” (compensated voltage and feedback current filtering), is modeled on a commonly used PHIL interfacing approach: design a simple compensator for the forward voltage path to achieve adequate $v_o \rightarrow v_o^*$ tracking, and then, if the closed-loop system is unstable (as was verified experimentally for this case study’s configuration), apply an interface stabilization technique, such as FCF. Here, we used a proportional-resonant controller with $K_v = k_p + \frac{2k_i\omega_c s}{s^2 + 2\omega_c s + \omega_0^2}$ where $k_p = 0.1$, $k_i = 200$, $\omega_c = 1$, and $\omega_0 = 2\pi 60$, and feed-forward gain, $K_{ff} = 0.7$, for the forward voltage path compensator. A first-order, low-pass FCF, $H_{fb} = \frac{1}{(1/2\pi 800)s + 1}$ is used. The second base case interface, “NVC” (no voltage compensation), models the case where no forward voltage path compensation is used ($K_v = 1$ and $K_{ff} = 1$) and the same low-pass FCF was used. This second interface is also commonly employed as it is one of the simplest stable PHIL interfaces to implement.

2) *Optimal (“Opt”) Interfaces*: Preliminary analysis of $\hat{i}_o^*$ when operating the HUT in open loop at 62 kW (62% of full power), shown in Fig. 3, revealed that the primary frequencies present in i_o^* were below 900 Hz. Thus, the HUT feedback performance range is identified as 60-900 Hz and $I_{TVE, 2, 15}$ will be used to assess the total normalized current TVE of the PHIL experiment. A measured (via current sensor datasheet characterization and knowledge of T_s) i_o^* to i_o time delay of $T_{fb} = 52.875 \mu\text{s}$ was also identified.

With this information, feedback current compensator designs— $H_{fb, sm}$, $H_{fb, smPL}$, and $H_{fb, tf}$ —were designed using the forms shown in Table I with parameters $T_{smith1} = 0.265 \text{ s}$, $T_{smith2} = 0.37 \text{ s}$, $T_{smPL} = 40e^{-6} \text{ s}$, $\omega_{smHF} = 4e^4 \text{ rad/s}$, $\omega_{fb} = 2\pi[60, 60 \cdot 5, 60 \cdot 7, 60 \cdot 55] \text{ rad/s}$, $\bar{H}_{fbFR} = [1 \angle 1.142^\circ, 1.05 \angle 5.99^\circ, 1.1 \angle 6.6^\circ, 1.05 \angle -30^\circ]$, and $O_{Hfb} = 2$. These parameters were selected to achieve $T_{fb} \cdot 60 \text{ Hz} \cdot 360^\circ = 1.1421^\circ$ of phase lead at the fundamental, appropriate phase lead (ωT_{fb}) at other selected frequencies within the HUT feedback performance range, roll-off at high frequencies,

and the closest fit (for H_{fb}). The transfer function fitting method resulted in $H_{fb,tf} = 0.48(s+4.59e4)(s+4836)/(s^2 + 1.78e^4s + 1.07e^8)$. Based on the results shown in Section IV-E1, $H_{fb,tf}$ was selected as the final H_{fb} design for the optimal PHIL interface.

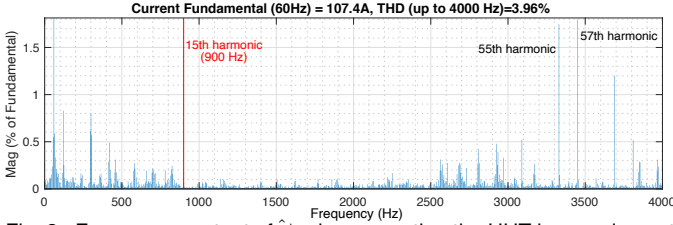


Fig. 3. Frequency content of $\hat{i}_o^*$ when operating the HUT in open loop at 62 kW. It can be seen that frequency content between 900-2,500 Hz is very small and then increases again above 2,500 Hz with peaks at the 55th and 57th harmonics.

For the synthesis of K_v , a performance weight for the closed-loop voltage error transfer function of the form $W_P = k_{DC}(k_p + \frac{2k_i\omega_c s}{s^2 + 2\omega_c s + \omega_0^2})(\frac{\omega_{lpf}}{s + \omega_{lpf}})^2$ was used with $k_{DC} = 12$, $k_p = 0.6$, $k_i = 3000$, $\omega_c = 0.01$, $\omega_0 = 2\pi 60$, and $\omega_{lpf} = 2\pi 2000$. This performance weight encourages high gain near the fundamental frequency and relatively low gain elsewhere. Here, k_p , k_i , and ω_c adjust the proportional gain, integral gain, and bandwidth, respectively, of the resonant peak at ω_0 ; k_{DC} changes the DC gain of W_P ; and ω_{lpf} controls the cut-off frequency for high-frequency roll-off. The input weight is designed to limit control effort at high frequencies and has the form $W_u = \frac{s+c_2\omega_w}{c_1s+\omega_w}$ with $c_1 = 0.01$, $c_2 = 0.1$, and $\omega_w = 0.1 \cdot 2\pi 60$. Here, c_1 and c_2 adjust the control effort gain at high and low frequencies, respectively. The two weighting functions used are shown in Fig. 4. The candidate K_{ff} based on the inverse of the plant is calculated to be $K_{ff} = 1/|P_{22}(j\omega)|_{\omega=\omega_0} = 0.91$ and provides an initial estimate to use. The feedforward gain $K_{ff} = 0.7$ was found to work best to achieve the desired output voltage scaling with similar response time performance in the experiment.

Using these weights and the process outlined in Section II-C, a K_v was synthesized successfully for each of the three candidate current feedback filters. That is, even though the design of H_{fb} changes, the same process of determining the weighted plant (and using the same weights) and optimally synthesizing a K_v is employed. A Bode plot of the K_v associated with $H_{fb,tf}$, which is the final optimal PHIL interface design used, is shown in Fig. 5. Note that the controller synthesis process outputs a high-order (235th order) controller because the minimum order obtainable will be the sum of the orders of the plant and the weights. This is then reduced to the 15th order controller shown in Fig. 5, which closely replicates the original controller, for practical implementation. K_v emphasizes performance near $\omega_0 = 2\pi 60$ as desired, but it also has another benefit: a notch is added to de-emphasize performance near $\omega = 2.01e^4$ rad/s—the resonant frequency of the power amplifier’s inductance and the HUT’s output filter capacitor. This notch is added by the optimal controller synthesis process and not because of a specific design in the performance weight, emphasizing the benefit of the approach.

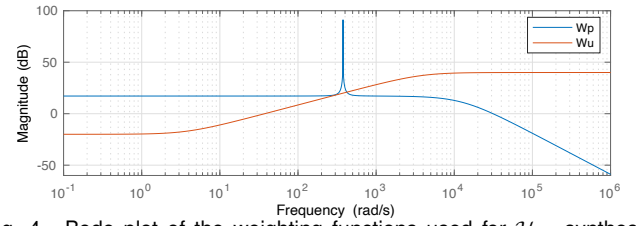


Fig. 4. Bode plot of the weighting functions used for $\mathcal{H}_\infty$ synthesis of K_v . W_P is designed to emphasize performance at the nominal frequency and W_u is designed to limit control effort to the bandwidth of the power interface.

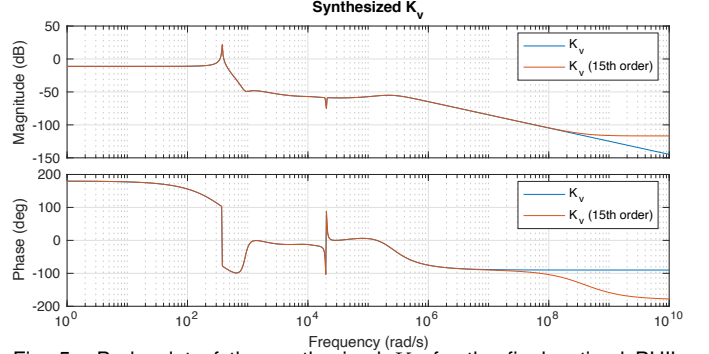


Fig. 5. Bode plot of the synthesized K_v for the final optimal PHIL interface design, which leverages current feedback filter $H_{fb,tf}$. K_v is originally 235th order, but is reduced to 15th order for implementation.

D. Stability Analysis

As described in Section II-D, as long as a controller can be synthesized, the closed-loop system is guaranteed to be stable; however, after controller model order reduction we additionally verified that the eigenvalues of $F_l(\tilde{P}, K_{v,15^{th} \text{ order}})$ are all in the strict left half plane, confirming closed-loop stability.

E. Experiment Results

Over 90 PHIL simulation runs were conducted to thoroughly validate the performance of the two base case PHIL interfaces (CVI and NVC) and three candidate optimal PHIL interfaces ($H_{fb,sm}$, $H_{fb,smPh}$, and $H_{fb,tf}$ with associated K_v) under a wide range of scenarios with varying HUT power, HUT power scaling factor (γ_i), and simulated grid impedance (Z_s) values. First, the relative performance of the three candidate optimal PHIL interfaces is examined to validate the best design of H_{fb} . Next, the selected optimal PHIL interface is compared against the two base case interfaces in 19 different testing scenarios to demonstrate the superior performance of the optimal interface using both steady-state and instantaneous waveform accuracy metrics (introduced in Section III-C).

1) *Identifying the best H_{fb} design for the optimal interface:* The relative performance of the three H_{fb} designs is evaluated by executing the same 12 PHIL simulation scenarios with the different H_{fb} designs (and their associated K_v) active and then evaluating normalized current TVE metrics $I_{TVE,2,15}$ and $I_{TVE,m}$ for $m = 2 \dots 15$. These metrics quantify the current tracking performance within the 900 Hz HUT feedback performance range identified. It can be seen from Fig. 6 that the $H_{fb,tf}$ design performed the best, with less than 3.5% TVE across all operating conditions, and is thus selected as H_{fb} for the optimal (“Opt”) PHIL interface.

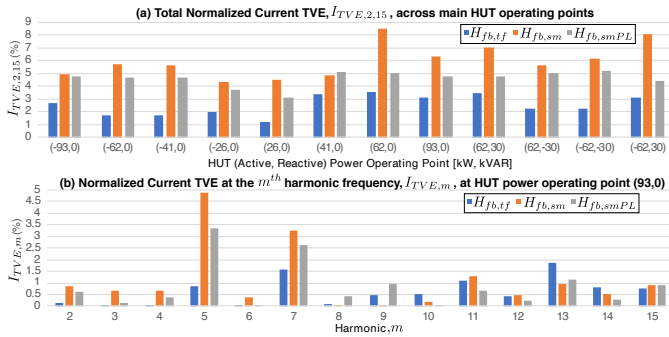


Fig. 6. Comparing the performance of the three H_{fb} designs for the optimal PHIL interface using (a) total normalized TVE measured at 12 different HUT power operating conditions and (b) normalized current TVE at individual harmonics at the near full power (93 kW, 0 kVAR) HUT power operating condition.

2) *Summary Steady-state Results:* Table V lists summary results from the many tests examining different combinations of Opt/CVI/NVC PHIL interface, HUT operating power, simulated grid interconnection impedance (Z_s), and scaling (the HUT power is scaled by γ_i to represent a larger capacity, S_{scl} , inverter in the simulated model) that were completed. Note that the CVI and NVC interfaces share the same current feedback filter and so metrics based on current only will be the same and are thus labeled CVI/NVC. The following conclusions can be made from Table V:

- 1) The optimal (“Opt”) interface offers improved tracking of all quantities (voltage, current, inst. power, active power, reactive power) versus the other interfaces. Improvements in instantaneous power tracking (see rIPTE), current tracking (see rICTE and $I_{TVE,2,15}$), and reactive power tracking (see RPTE) are particularly significant (i.e., the Opt interface has 5-10X lower error). The excellent tracking performance of the optimal PHIL interface (all quantities are tracked within 1%) ensures a reliable and accurate PHIL simulation.
- 2) The CVI and NVC interfaces have 3%–12% RPTE, whereas the optimal interface RPTE is within 0.1% for all cases. This large difference occurs because the Opt interface precisely compensates for delay at the fundamental frequency, while the CVI and NVC interfaces do not (see FCATE). The CVI and NVC interfaces also have inferior current tracking at other frequencies, as reflected in higher $I_{TVE,2,15}$ and as can be observed in Fig. 8.
- 3) The rICTE based on the unfiltered current (rICTE-NoFilt) is larger than the base rICTE (based on the filtered current) because it takes into account instantaneous current error at all frequencies, even those beyond BW_{sys} (such as the 55th and 57th harmonics in Fig. 3) which are not significant because accurate current tracking cannot be expected beyond the PHIL simulation bandwidth.
- 4) Under a wide range of conditions with varying HUT power factor, power scaling factor (S_{scl}), and simulated grid impedance (Z_s) values, high accuracy is demonstrated and the variations in testing parameters do not lead to much impact on performance. This confirms that the optimal PHIL interface design is robust to varying model conditions, performing well even though the interface was

synthesized based on a plant model with fixed S_{scl} , Z_s , Y_{hut} , etc. values.

3) *Detailed Dynamic Results:* Detailed performance results from a 41-kW to 93-kW step change in HUT active power set point are shown in Fig. 7 and Fig. 8 (magnified view). These figures emphasize that the optimal interface both:

- 1) fully compensates for phase lag (achieves nearly zero phase lag vs. 5+ degrees of phase lag for the CVI case), which contributes to the significantly better reactive power tracking demonstrated in Table V; and
- 2) has significantly improved current tracking performance, both when considering current error at all frequencies (Opt-NoFilt) and frequencies within the PHIL simulation bandwidth (Opt). The Opt interface has nearly zero current tracking error throughout the transition while the CVI interface filters out many of the higher frequency components present, resulting in higher error.

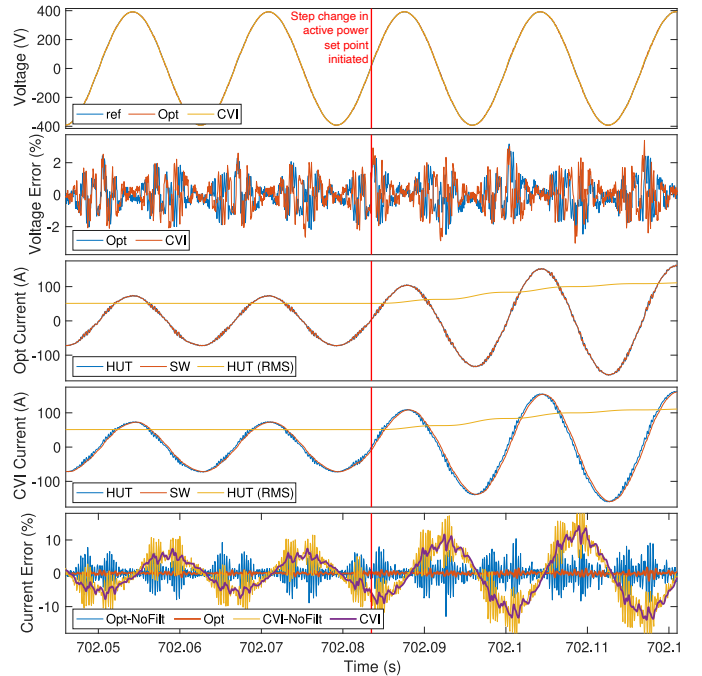


Fig. 7. Phase A instantaneous voltage, voltage error (IVTE), current (from the Opt vs. CVI interfaces), and current error (ICTE) throughout a 41 kW to 93 kW change in HUT active power set point, which is initiated near $t = 702.083$ s.

V. CONCLUSION

In this article, we developed a novel approach for the optimal design of PHIL interfaces and showed how to apply a widely applicable method to a PHIL simulation case study. We demonstrated that this optimal design approach can simplify the process of developing high-accuracy PHIL interfaces—whereas common approaches involve multiple steps of manual compensation and stabilization design—by using a modern control design framework, specifying performance bounds, and then automatically synthesizing an optimal controller. This considerably simplifies the design of a stabilizing PHIL interface compensator by removing the need to iterate over controllers and allowing explicit definition of accuracy objectives, rather than leaving performance to subjective measures with only a posteriori evaluation possible. In the case

TABLE V.
SUMMARY TEST RESULTS

Varying		Test Conditions				Tracking Error Metric (%)												Fund. Current Angle Diff.						
		HUT (kVA)	Model (MVA)	Inst. Power rIPTE			Inst. Voltage rIVTE			Inst. Current rICTE		Current TVE $I_{TVE,2,15}$		Active Power APTE			Reactive Power RPTE			FCATE (deg)				
P	P	Q	S_{scl}	Z_s	Opt	CVI	NVC	Opt	CVI	NVC	Opt	CVI	NVC	Opt	CVI	NVC	Opt	CVI	NVC	Opt	CVI	NVC		
	-93	0	2.5	min	0.38	3.37	2.13	0.65	0.70	2.78	0.40	6.62	2.96	7.11	2.73	25.15	0.17	0.67	1.06	-0.02	-8.63	-12.08	-0.01	5.34
	-62	0	2.5	min	0.40	3.38	2.15	0.65	0.68	2.78	0.50	6.64	4.11	7.52	1.73	33.25	0.11	0.44	0.70	-0.01	-5.75	-8.05	-0.01	5.34
	-41	0	2.5	min	0.47	3.39	2.19	0.64	0.68	2.78	0.65	6.67	5.72	8.34	1.75	25.81	0.07	0.35	0.55	-0.01	-3.83	-5.36	-0.01	5.34
	-26	0	2.5	min	0.61	3.42	2.26	0.64	0.67	2.77	0.98	6.75	6.75	10.10	1.98	23.99	0.05	0.22	0.34	0.01	-2.40	-3.36	-0.01	5.34
	26	0	2.5	min	0.47	3.43	2.23	0.65	0.70	2.78	0.64	6.73	5.53	8.38	1.25	22.15	-0.05	-0.08	-0.15	0.01	2.44	3.42	-0.01	5.35
	41	0	2.5	min	0.44	3.37	2.16	0.70	0.72	2.79	0.57	6.68	4.56	7.86	3.39	28.08	-0.08	-0.20	-0.34	0.01	3.87	5.42	-0.01	5.35
	62	0	2.5	min	0.40	3.34	2.13	0.68	0.73	2.79	0.46	6.66	3.43	7.35	3.56	25.68	-0.12	-0.39	-0.63	0.01	5.79	8.10	-0.01	5.34
	93	0	2.5	min	0.38	3.32	2.10	0.70	0.73	2.79	0.40	6.64	2.57	7.03	3.13	29.31	-0.17	-0.54	-0.88	0.01	8.65	12.11	-0.01	5.35
	(P, Q)	P	Q	S_{scl}	Z_s	Opt	CVI	NVC	Opt	CVI	NVC	Opt	CVI	NVC	Opt	CVI	NVC	Opt	CVI	NVC	Opt	CVI	NVC	
62		-30	2.5	min	0.46	4.09	3.94	0.67	0.71	2.79	0.48	6.66	3.69	7.41	3.49	29.56	-0.12	-3.22	-4.59	-0.05	5.60	7.81	-0.01	5.35
62		-30	2.5	min	0.43	3.77	3.20	0.69	0.73	2.79	0.38	6.64	2.51	6.99	2.27	32.17	-0.11	2.51	3.44	0.07	5.97	8.41	-0.01	5.35
-62		-30	2.5	min	0.43	4.11	3.98	0.64	0.67	2.78	0.36	6.63	2.90	7.12	2.22	35.09	0.12	3.30	4.71	0.05	-5.56	-7.74	-0.01	5.35
-62		-30	2.5	min	0.49	3.82	3.20	0.64	0.68	2.78	0.54	6.65	4.54	7.79	3.17	26.99	0.11	-2.42	-3.30	-0.07	-5.94	-8.36	-0.01	5.35
-77		0	2.5	min	0.39	3.36	2.13	0.65	0.69	2.78	0.43	6.64	3.34	7.25	2.49	25.31	0.14	0.54	0.86	-0.01	-7.21	-10.10	-0.01	5.35
-77		0	3	min	0.38	3.37	2.15	0.67	0.67	2.77	0.39	6.63	3.28	7.24	2.03	24.95	0.14	0.62	0.97	-0.02	-7.20	-10.08	-0.01	5.35
-77		0	4.8	min	0.38	3.37	2.13	0.64	0.68	2.77	0.45	6.63	3.16	7.22	1.87	31.34	0.14	0.54	0.87	-0.01	-7.20	-10.08	-0.01	5.35
-77		0	5.5	min	0.39	3.36	2.12	0.64	0.69	2.78	0.46	6.62	3.08	7.20	1.89	26.52	0.14	0.50	0.81	-0.01	-7.19	-10.07	-0.01	5.35
Z_s		P	Q	S_{scl}	Z_s	Opt	CVI	NVC	Opt	CVI	NVC	Opt	CVI	NVC	Opt	CVI	NVC	Opt	CVI	NVC	Opt	CVI	NVC	
	62	0	1	min	0.38	3.34	2.11	0.69	0.73	2.79	0.47	6.66	3.54	7.36	3.35	30.74	-0.12	-0.29	-0.49	0.01	5.79	8.10	-0.01	5.35
	62	0	1	mid	0.39	3.35	2.13	0.70	0.72	2.79	0.44	6.66	3.45	7.34	3.30	25.22	-0.12	-0.38	-0.61	0.01	5.79	8.11	-0.01	5.35
	62	0	1	max	0.39	3.35	2.13	0.69	0.72	2.79	0.48	6.66	3.33	7.33	3.40	29.42	-0.12	-0.32	-0.54	0.01	5.80	8.12	-0.01	5.35

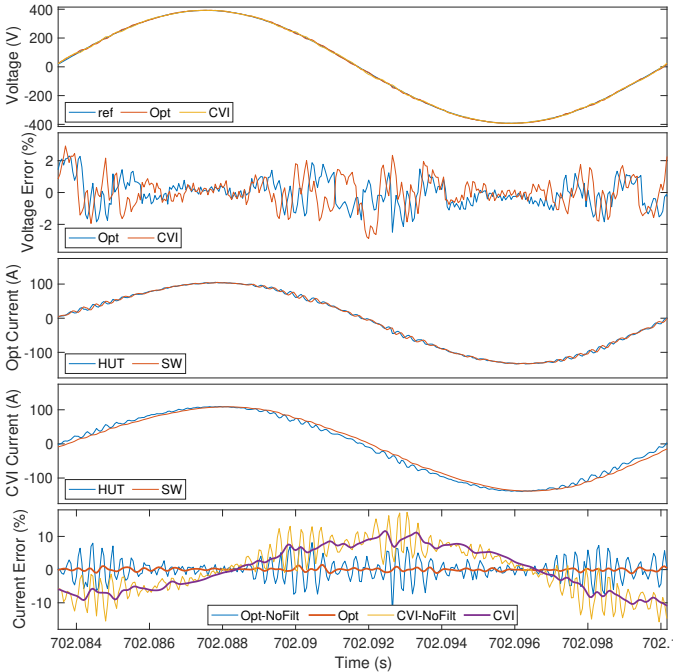


Fig. 8. Magnified view of Fig. 7, beginning at the red cursor indicated in Fig. 7. Note the significantly better tracking (phase and bandwidth) shown in the Opt Current vs. CVI Current plots.

study, the bandwidth and accuracy of the PHIL simulation results were compared when using the optimal PHIL interface compensation design versus commonly used interface design approaches, and significant performance improvements were shown for the optimal approach. We also introduced a practical framework and metrics for verifying the accuracy of the PHIL simulation results that provides a quantitative measure of how accurate a particular simulation result is without relying on relative comparisons to potentially inaccurate models or previous simulation results. This accuracy evaluation method provides a valuable means for PHIL practitioners and researchers to easily identify a particular simulation's absolute accuracy and compare results from different simulations on a common basis.

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