

Robust and Optimal Single-loop Voltage Controller for Grid-forming Voltage Source Inverters

Soham Chakraborty, Sourav Patel, and Murti V. Salapaka

Department of Electrical and Computer Engineering

University of Minnesota

{chakr138, patel292, murtis}@umn.edu

Abstract—Design and implementation of an optimal and robust single-loop voltage controller is proposed for single-phase grid-forming voltage source inverter (VSI). The objective of the proposed controller is to have good reference tracking and disturbance rejection. Uncertain nature of loads can significantly alter system's behavior, especially during heavily loaded conditions, and impose an uncertainty in the dynamic model. This deteriorates the robustness of the controller severely. $\mathcal{H}_\infty$ -based controller design is proposed in this article to address this issue. The required objectives of the optimal controller are formulated after modeling the loads as uncertain element of the control system. Time-domain MATLAB/SIMULINK-based simulation study substantiates the fact that the resulting controller exhibits superior robustness in performance during varying loading conditions of VSI than that of the conventional multi-loop control architecture. OPAL-RT based controller hardware-in-the-loop (CHIL) simulations with low-cost controller are conducted to validate the computational footprint of the resulting controller.

Index Terms— $\mathcal{H}_\infty$ loop shaping, multiplicative uncertainty, robust control, voltage controller, voltage source inverter,

I. INTRODUCTION

During islanded mode of operation of AC microgrid, grid-forming voltage source inverters (VSI) play an essential role by maintaining a stable voltage and frequency of the network and supplying uninterrupted power to the loads in the absence of a stiff distribution grid. Both centralized (*master-slave*) and decentralized (*droop-based*) *Level-1* control layer architecture have been proposed in order to meet the uninterrupted power supply to the loads in the network via generating a voltage reference for the *Level-0* control layer [1]. In *Level-0* control layer, a voltage controller is required to be designed for each grid-forming VSI so that the output voltage waveform of each VSI tracks the respective voltage reference signal [2].

Designing the voltage controller is essentially a multi-objective task. The design needs to primarily guarantee perfect reference tracking and good disturbance rejection which results in an output voltage with good regulation and low harmonic distortion in presence of various linear and non-linear loads. Additionally, the controllers are required to provide compensation to dynamic variations of the output current and improve the dynamic response [3]. It is also found that the unknown nature of the output loads can significantly alter the system behavior, especially during heavily loaded condition of VSI, that deteriorates the transient performance severely [4]. The controller is required to perform all the aforementioned multi-objective tasks under output load uncertainties.

As a result, requirement of robust performance of the voltage controller warrants an essential criterion during design stage.

Numerous voltage control strategies are proposed in the literature during past decades for grid-forming VSIs. Most of the earlier control techniques are based on linear control theory with a single voltage control-loop scheme [5]. To further enhance the disturbance imposed by variations in input voltage and output current, a non-linear feed-forward loop is added in [6]. However, single-loop classical controllers experience poor transient response and limited stability margins [7]. To overcome these drawbacks, multiple-loop proportional-resonant (PR) and proportional-integral-differential (PID)-based classical control methods are proposed in [7]–[10]. This common architecture has an internal current negative feedback loop, commanded by the error signal of the outer voltage regulation loop [3]. By introducing the inner current loop, the poles of the resonant LC filter can be decoupled to compensate the non-idealities of the inductor. Moreover, it facilitates an inherent over-current protection of the VSI. However, having an inner-loop current controller requires more sensors that increases the overall cost [11]. Moreover, classical controllers lack robustness in performance with output load uncertainties [9]. In [12]–[14], a lower order controller is designed using $\mathcal{H}_\infty$ methodology by removing the higher order part of the internal model using repetitive control technique. However, in these approaches load uncertainty is not taken into account. A robust tuning strategy for PID-based double-loop lag-lead compensator for VSI is proposed in [15]. $\mathcal{H}_\infty$ -based methodology is further explored in [16]–[19] in order to design an optimal controller for VSIs with linear and non-linear load disturbances. However, both these works inherently adapt the multi-loop structure for voltage controller and load uncertainty is not considered during design. In [20], a sliding-mode control-based design for inner current loop and a mixed $\mathcal{H}_2/\mathcal{H}_\infty$ -based optimal design for outer voltage loop is proposed. A very similar design is proposed in [21] where linear matrix inequality (LMI)-based linear quadratic regulator (LQR) for inner current loop and mixed $\mathcal{H}_2/\mathcal{H}_\infty$ -based design for outer voltage loop are employed. Both these designs improve the transient response significantly in presence of uncertain filter parameters at the cost of added complexity in controllers. Moreover, uncertainty imposed by output loads is not taken into consideration while designing the controllers. [22] provides a robust optimal state-feedback controller based

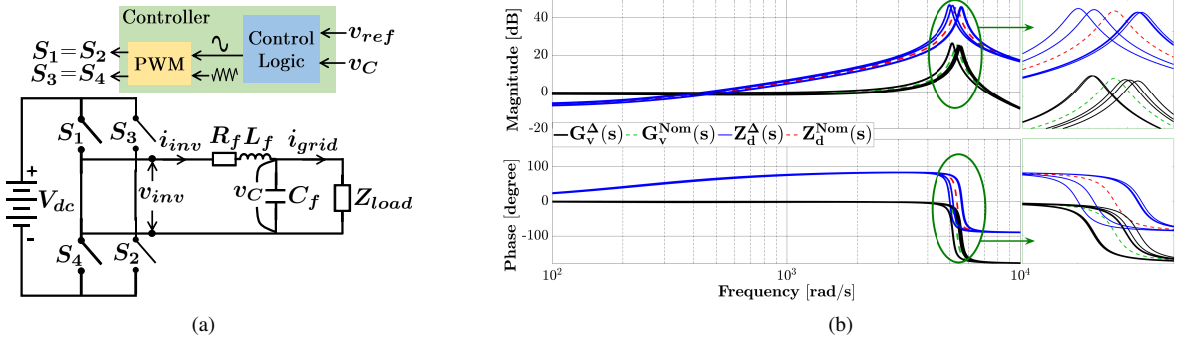


Fig. 1. Description of the system with (a) the schematic of single-phase grid-forming VSI, (b) variation of plant dynamics model due to uncertain load.

on the integration of optimal output regulation theory and back-stepping method where load is treated as a uncertain element. However, the impact of non-linear loads (various harmonic components) is not considered in this work. The primary contributions of this article are as follows:

- 1) A simple robust and optimal (single-loop, low-cost) voltage controller for *Level-0* control layer is proposed that can address the aforementioned limitations along with taking into account the uncertainties in load variations.
- 2) It facilitates lower requirements of sensor measurements as opposed to other works in the literature without compromising in voltage regulation and disturbance rejection while guaranteeing robust performance.

Time-domain MATLAB/SIMULINK-based simulation as well as OPAL-RT CHIL-based simulation with low-cost controller are performed in the validation stage of the proposed control.

II. PROBLEM FORMULATION

A. Architecture of Grid-forming VSI

A single-phase grid-forming VSI terminated by a load, Z_{Load} , is shown in Fig. 1(a). The VSI is composed of a dc bus voltage, V_{dc} , four switching devices, S_1 - S_4 , and an LC filter with L_f , C_f as filter inductor and capacitor respectively. R_f is the equivalent series resistance (ESR) of L_f capturing parasitic element. The controller along with sinusoidal PWM switching technique generates the switching signals that result the output voltage. The dynamics of the VSI are described as:

$$L_f \frac{d\langle i_{inv} \rangle}{dt} + R_f \langle i_{inv} \rangle = \langle v_{inv} \rangle - \langle v_C \rangle, \quad (1)$$

$$C_f \frac{d\langle v_C \rangle}{dt} = \langle i_{inv} \rangle - \langle i_{grid} \rangle, \quad (2)$$

where $\langle \cdot \rangle$ signifies the average values of the corresponding variable over one switching cycle (T_s) [3]. Combining (1) and (2) and taking Laplace transformation, the open-loop output voltage dynamics of the grid-forming VSI is given as:

$$V_C(s) = G_{inv}(s)V_{inv}(s) - G_i(s)I_{grid}(s), \quad (3)$$

where

$$G_{inv}(s) = \frac{1}{L_f C_f s^2 + R_f C_f s + 1},$$

$$G_i(s) = \frac{L_f s + R_f}{L_f C_f s^2 + R_f C_f s + 1}.$$

B. Load Characteristics and Modeling

Characterizing the nature of the load is essential in the process of designing the controller. In this work, the load is modeled by a parallel combination of two components. First component is an admittance, $Y_L(s)$, with unknown R and L elements, and can be defined as:

$$Y_L(s) := [1 + \Delta(s)]Y_L^N(s),$$

where, $Y_L^N(s)$ is a frequency dependent weighting function, capturing the nominal behavior, and defined as:

$$Y_L^N(s) := \frac{1}{L_L^N s + R_L^N}.$$

A normalized dynamic LTI uncertainty, $\Delta(s)$, is defined to capture the uncertain behavior of load change such that

$$\|\Delta(s)\|_\infty \leq 1.$$

The value of L_L^N and R_L^N can be selected as $R_L^N = V_{rated}^2 / P_{rated}$ and $L_L^N = V_{rated}^2 / (\omega_o Q_{rated})$, where V_{rated} , P_{rated} , Q_{rated} and ω_o are the rated output voltage, active, reactive power of the grid-forming VSI and nominal frequency of the network respectively. Another component of loads is a parallel combination of current sources consisting of both fundamental and harmonic components [23] and defined as

$$I_d(s) := \sum_h I_{d,h}(s), \quad [h \text{ is odd}].$$

Therefore, Z_{Load} of Fig. 1(a) can be characterized as

$$I_{grid}(s) = Y_L(s)V_C(s) + I_d(s)$$

$$= [1 + \Delta(s)]Y_L^N(s)V_C(s) + \sum_h I_{d,h}(s). \quad (4)$$

Remark. Multiplicative uncertainty in $Y_L(s)$ is used to shape the “worst-case” yet allowable output admittance of the grid-forming VSI. The exogenous disturbance signal, $I_d(s)$, captures the presence of non-linear loads as shown in Fig. 2(a).

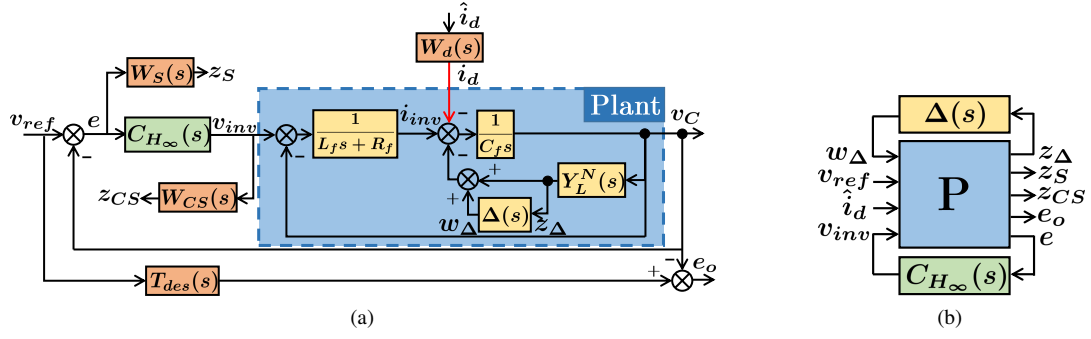


Fig. 2. $\mathcal{H}_\infty$ -based controller synthesis, (a) the closed-loop control system with selected weighting transfer functions, (b) general control configuration.

C. Impact of Load Uncertainty

Combining (3) and (4), system's dynamic equation becomes

$$V_C(s) = G_v^\Delta(s) V_{inv}(s) - Z_d^\Delta(s) I_d(s). \quad (5)$$

where,

$$G_v^\Delta(s) = \frac{G_{inv}(s)}{1 + G_i(s) Y_L(s)}, \quad Z_d^\Delta(s) = \frac{G_i(s)}{1 + G_i(s) Y_L(s)}.$$

Clearly uncertainty in $Y_L(s)$ imposes uncertainty in both $G_v^\Delta(s)$ and $Z_d^\Delta(s)$ as illustrated in Fig. 1(b). It can be observed that the unknown load across VSI causes significant change in the plant dynamics, especially the effective resonant frequency of the system. This deteriorates the robust performance of the controller severely as well as overall system stability [4].

III. PROPOSED SOLUTION

A. Objectives of the Designed Controller

The objective is to design a feedback control law through controller, $C_{H\infty}(s)$ as shown in Fig. 2(a), which generates a control signal, v_{inv} , such that, i) v_C tracks v_{ref} , ii) effects of i_d on v_C is attenuated, iii) v_{inv} satisfies bandwidth limitations, and iv) v_C recovers quickly after any sort of transients. Moreover, all aforementioned objectives need to be achieved with load uncertainty. In other words, it is necessary to provide the controller with enough robustness to deal with system uncertainty caused by load variation. These objectives are derived from acceptable standards on microgrid operation, IEEE Std-2030 [24], and power quality, IEEE Std-519 [25].

B. Design Procedure of the $\mathcal{H}_\infty$ -based Controller

$\mathcal{H}_\infty$ -based controller design provides a framework for addressing multiple objectives. Here, the design is based on the system structure presented in Fig. 2(a) where user-defined weighting transfer functions, $W_S(s)$, $W_{CS}(s)$, $W_d(s)$ and $T_{des}(s)$, are selected based on the aforementioned requirements. The brief guidelines for designing the weighting transfer functions are provided below.

1) *Selection of $W_S(s)$* : To shape the sensitivity transfer function, the weighting function, $W_S(s)$ is introduced so that

- the tracking error at ω_o is extremely low,
- the LC resonance of VSI is actively damped,

$W_S(s)$ is modeled to have peaks at ω_o and LC resonant frequency, ω_{res} , with a overall gain $k_{S,1}$. Hence,

$$W_S(s) = k_{S,1} \left[\frac{s^2 + 2k_{S,2}\zeta\omega_o s + \omega_o^2}{s^2 + 2\zeta\omega_o s + \omega_o^2} \right] \left[\frac{s^2 + 2k_{S,3}\zeta\omega_{res} s + \omega_{res}^2}{s^2 + 2\zeta\omega_{res} s + \omega_{res}^2} \right],$$

where, $k_{S,2}$ and $k_{S,3}$ are selected to exhibit peaks and ζ takes care of the off-nominal system frequency.

2) *Selection of $W_{CS}(s)$* : $W_{CS}(s)$ is designed to suppress high-frequency control effort to shape the performance of v_{inv} . Hence, it is designed as high-pass filter with cut-off frequency at switching frequency and ascribed the form:

$$W_{CS}(s) = \frac{s + k_{CS,1}\omega_o}{s + k_{CS,2}\omega_o}, \text{ where } k_{CS,1} \ll k_{CS,2}.$$

3) *Selection of $W_d(s)$* : $W_d(s)$ emphasizes the expected disturbances at ω_o and at different harmonic frequencies imposed by i_d and emphasized by exogenous signal $\hat{i}_d$. It is based on the assumption that the load current comprises fundamental, 3rd, 5th, 7th, 9th, 11th and 13th harmonics. Hence, it is designed by a low-pass filter with peaks at selected frequencies. The resulting function is obtained as

$$W_d(s) = \prod_{h=1,3,\dots,13} \frac{s^2 + 2k_{d,h}\zeta h\omega_o s + h^2\omega_o^2}{s^2 + 2\zeta h\omega_o s + h^2\omega_o^2},$$

where, the values of $k_{d,h}$ are selected based on the THD standards mentioned in IEEE Std-519 [25].

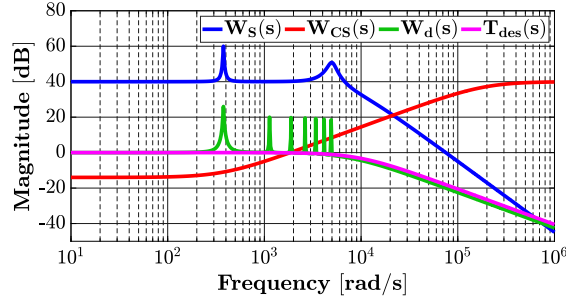
4) *Selection of $T_{des}(s)$* : To emphasize on the desired performance of the closed-loop system, a performance bound is designed with a typical first-order transfer function specified by the parameters k_B , ω_B^* in the following expression.

$$T_{des}(s) = k_B \frac{\omega_B^*}{s + \omega_B^*}.$$

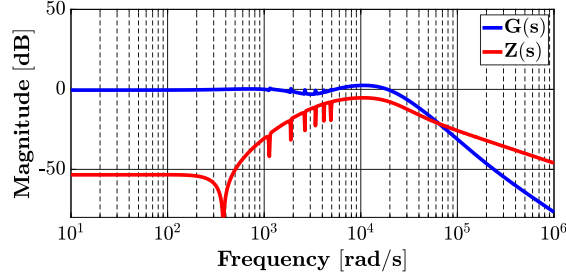
Clearly, the desired output response is decided based on the selection of ω_B^* , which is determined by the requirement of speed of response. Desired bandwidth of at least 10 times of ω_o , decides the value of ω_B^* with k_B as overall gain.

C. Problem Formulation and Resulting Optimal Controller

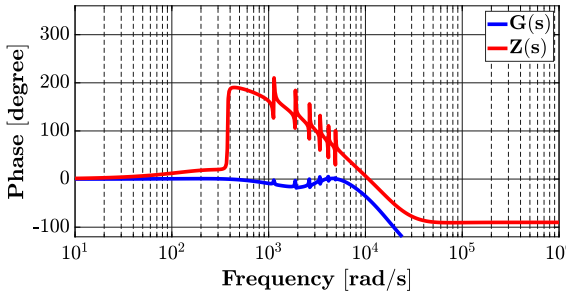
The Bode plots of the selected weighting transfer functions in this work are shown in Fig. 3(a). The $\mathcal{H}_\infty$ optimal problem



(a)



(b)



(c)

Fig. 3. Bode plots of (a) magnitudes of weighting transfer functions, (b) magnitudes of $G(s)$ and $Z(s)$ and (c) phase of $G(s)$ and $Z(s)$.

is formulated to generate a feedback control law with controller, $C_{H_\infty}(s)$, stated as:

$$V_{inv}(s) = C_{H_\infty}(s)[V_{ref}(s) - V_C(s)]. \quad (6)$$

As a result, the closed loop system equation can be found by combining (5) and (6) and can be written as

$$V_C(s) = G(s)V_{ref}(s) - Z(s)I_d(s), \quad (7)$$

where

$$G(s) = \frac{G_v^\Delta(s)C_{H_\infty}(s)}{1 + G_v^\Delta(s)C_{H_\infty}(s)}, \quad Z(s) = \frac{Z_d^\Delta(s)}{1 + G_v^\Delta(s)C_{H_\infty}(s)}.$$

Therefore, it is equivalent to state that the optimal controller is required to be designed such that

$$G(s)|_{s=j\omega_o} \approx 1\angle 0^\circ, \\ Z(s)|_{s=jh\omega_o} \ll 1 \quad [h = 1, 3, 5, 7, 9, 11, 13].$$

The control system of Fig. 2(a) can be realized as a general control configuration as shown in Fig. 2(b) [26]. It has a

TABLE I
VSI PARAMETERS FOR MATLAB/SIMULINK AND CHIL SIMULATION

VSI Parameter	Value
Rated RMS Output Voltage	220 (V)
Rated Output Frequency (ω_o)	$2\pi 60$ (rad/s)
DC Link Voltage (V_{dc})	500 (V)
Switching Frequency	20 (kHz)
LC Filter Inductance (L_f)	2 (mH)
LC Filter Capacitance (C_f)	20 (μ F)
Rated Output Power	2 (kVA)

generalized MIMO plant, P , containing nominal plant models defined as $G_v^{Nom}(s)$, $Z_d^{Nom}(s)$, $W_s(s)$, $W_{CS}(s)$, $W_d(s)$ and $T_{des}(s)$ with exogenous input signal $w := [v_{ref} \ i_d]^\top$ and output signals $z := [z_s \ z_{CS} \ e_o]^\top$. The controller, $C_{H_\infty}(s)$ has input feedback signal, e , and output control signal, v_{inv} . The uncertainty function, $\Delta(s)$, with input signal, z_Δ , and output, w_Δ is represented using upper linear fractional transformations [26]. The goal is to synthesize the stabilizing controller, $C_{H_\infty}(s)$, that satisfies the following:

$$\|T_{w \rightarrow z}\|_\infty < 1. \quad (8)$$

Remark. Small-gain theorem states that the accomplishment of (8) together with $\|\Delta(s)\|_\infty \leq 1$ guarantees the robust stability of the closed-loop system. [26]

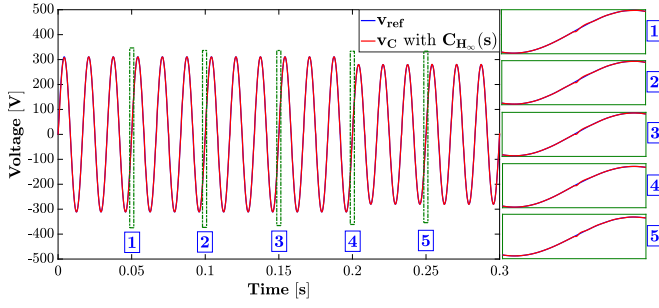
Using γ -iteration algorithm provided in [26] (the state-space solution approach via solving two algebraic Riccati equations), the synthesis of optimal controller is achieved by means of *hinfsyn* command of MATLAB toolbox. Usually H_∞ -control algorithms produce controllers of higher order and model reduction becomes essential to design a low order implementable controller. It is achieved by using balanced truncation method removing modes faster than the switching frequency. The resulting controller, $C_{H_\infty}(s)$, is of the order of 17 which is higher only by 3 orders than that of conventional PR controller with up to 13th order harmonic compensators. Fig. 3(b) and 3(c) corroborate the accomplishment of the objectives by the resulting optimal controller. Moreover, the optimal controller along with the plant results $\|T_{w \rightarrow z}\|_\infty = 0.77$ that makes the closed-loop system robust stable. Moreover, robust stability margin is verified by *robstab* command of MATLAB.

IV. RESULTS

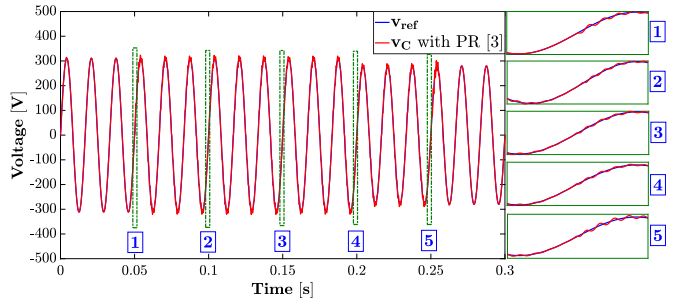
SIMULINK/MATLAB and CHIL-based simulation studies are carried out for validation. The system parameters used in both the stages are tabulated in Table I. A combination of impedance type and current source type load models are used. However, for closer proximity with practical scenarios, a DC-drive motor load is also considered along with the others and the modelling is followed as mentioned in [23], [27].

A. Simulation Results and Performance Comparison

For the purpose of performance comparison, conventional multi-loop-based classical outer PR-based voltage controller



(a)



(b)

Fig. 4. Simulation results, (a) waveform of reference voltage and output voltage with proposed controller, (b) with conventional PR-based controller [3].

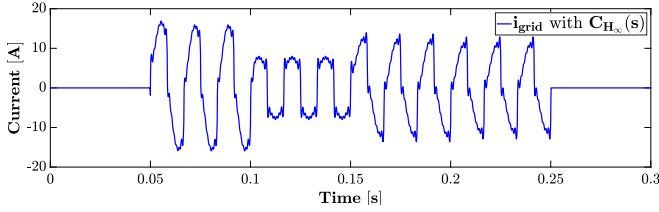


Fig. 5. Simulation results of output load current waveform of VSI.

TABLE II
REFERENCE TRACKING AND THD PERFORMANCE COMPARISON

Simulation Study	Controller Type	Magnitude Error (%)	Phase Error (%)	THD (%)
SIMULINK	$C_{H_\infty}(s)$ -based	± 0.74	± 1.39	0.41
	PR-based [3]	± 1.41	± 2.92	1.39
CHIL	$C_{H_\infty}(s)$ -based	± 0.97	± 1.89	0.57

and inner PI-based current controller is considered for the time-domain simulation. [3] provides an elaborated guidelines for designing the classical PR and PI based multi-loop voltage controller for grid-forming VSI with enough gain and phase margins. In this work, the guidelines are followed in order to possess a fair comparative study. PI-based inner loop is designed to have phase margin (PM) $\geq 60^\circ$ and gain margin (GM) ≥ 40 dB with bandwidth ≥ 5 kHz. Similarly, PR-based outer loop is designed to have PM $\geq 45^\circ$ and GM ≥ 40 dB with bandwidth ≥ 5 kHz. The following sequence of events is used in the MATLAB/SIMULINK-based validation stage.

- VSI is in no-load condition until $t = 0.05$ s.
- At $t = 0.05$ s, there is a transition from no-load to full-load and stays at full-load condition until $t = 0.1$ s.
- At $t = 0.1$ s, reactive power drops to 0 until $t = 0.15$ s.
- At $t = 0.15$ s, both real and reactive power change.
- At $t = 0.2$ s, v_{ref} drops and stays until $t = 0.25$ s.
- At $t = 0.25$ s, VSI is switched to no-load condition.

The output voltage waveform of VSI, v_C , during the time-domain events with both proposed $\mathcal{H}_\infty$ -based and conventional-multi-loop-based voltage controller are shown in Fig. 4(a) and Fig. 4(b). The enlarged portions in these figures

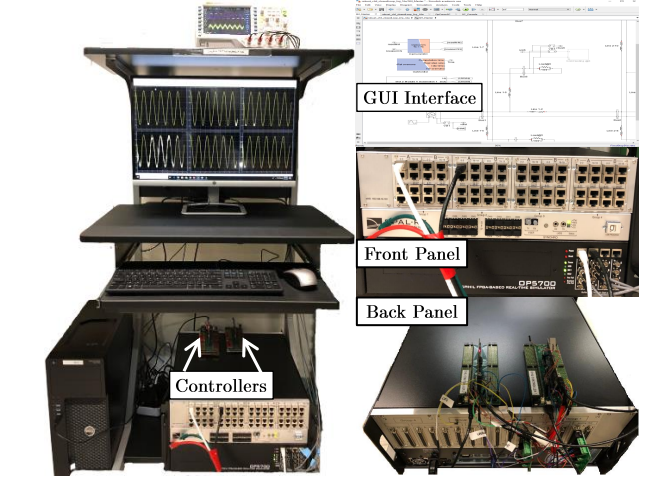


Fig. 6. OPAL-RT based hardware-in-the-loop simulation platform with Texas Instruments Delfino TMS320F28379D controller board.

are illustrating the transient behaviors during aforementioned situations. The results substantiate the fact that the proposed $\mathcal{H}_\infty$ -based controller exhibits superior robustness in performance than the multi-loop controller with varying loading conditions. THD of v_C with proposed controller is much smaller than the multi-loop controller with highly non-linear loads (output current is illustrated in Fig. 5). Finally, Table II corroborates the superiority of the proposed controller in reference tracking and disturbance rejection in compare with the classical multi-loop PR-based voltage controller at the cost of increasing the order of controller only by 3.

B. CHIL Simulation Results

The computational footprint of the proposed $\mathcal{H}_\infty$ -based controller, while implemented in a real low-cost micro-controller board, is an essential check for further validating the performance. Therefore, controller hardware-in-the-loop (CHIL)-based simulation studies are also conducted on OPAL-RT real-time simulator with the proposed $\mathcal{H}_\infty$ -based controller realized on a low-cost Texas-Instruments TMS28379D Delfino controller board as shown in Fig. 6. In similar way, four events are emulated in the OPAL-RT platform and are enlisted as:

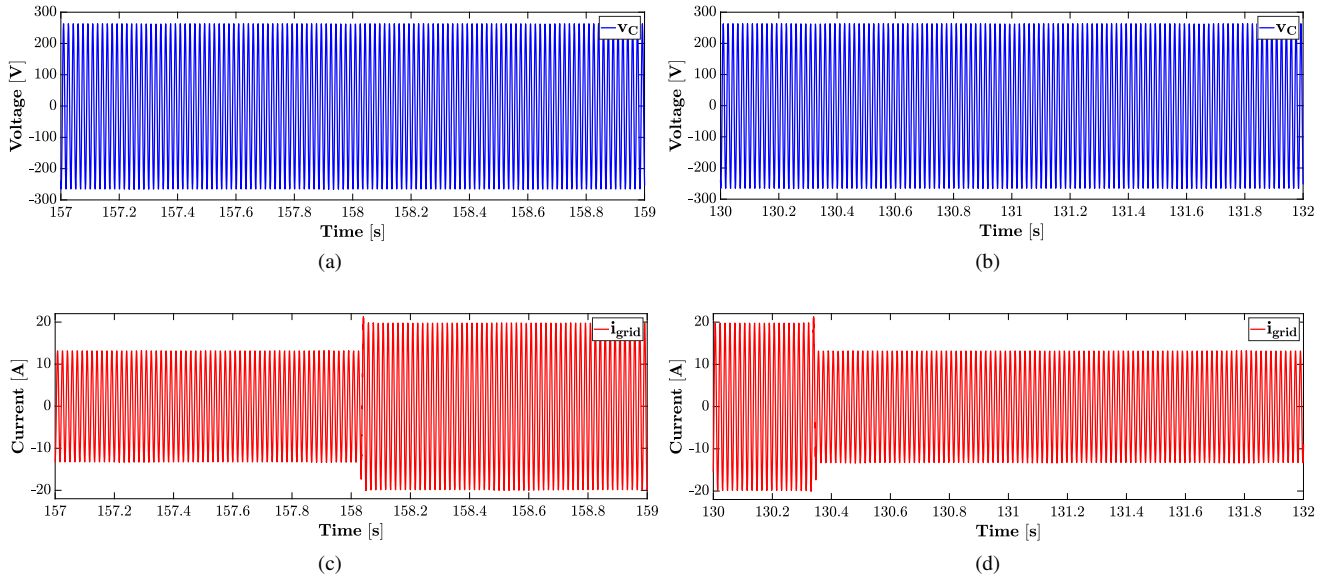


Fig. 7. CHIL simulation results of output voltage waveform of VSI with (a) CASE-1: sudden rise in output current at $t = 158.05$ s and (b) CASE-2: sudden fall in output current at $t = 130.35$ s with proposed controller, (c) rise in output current in CASE-1, (d) fall in output current in CASE-2.

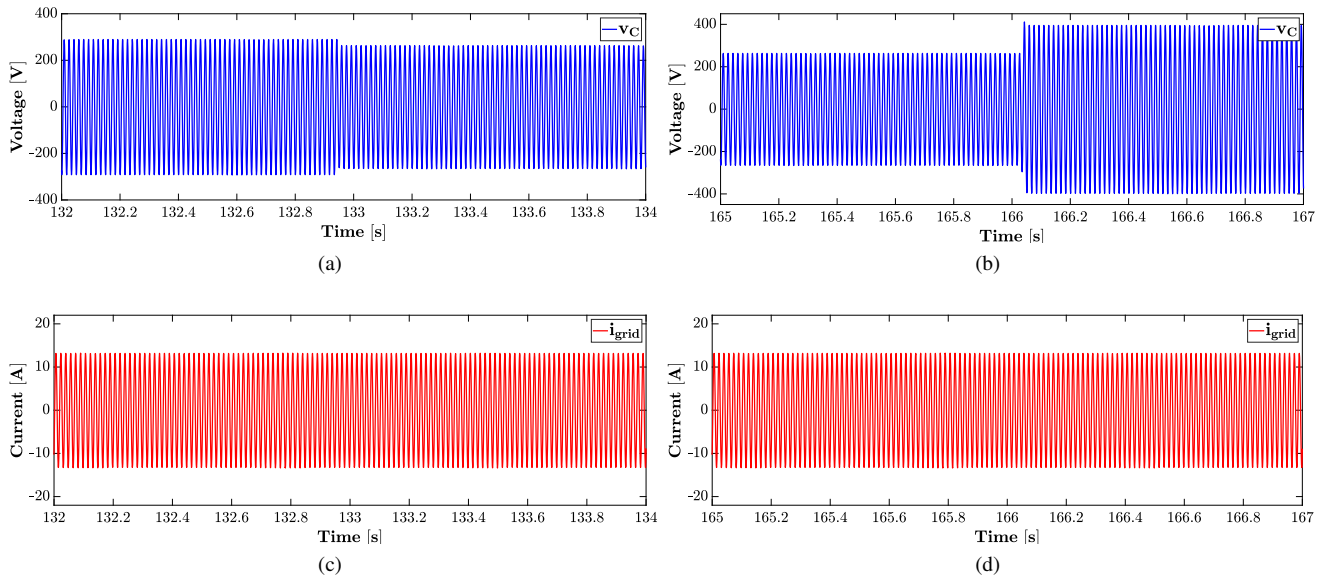


Fig. 8. CHIL simulation results of output voltage waveform of VSI with (a) CASE-3: sudden fall in output voltage reference signal at $t = 132.95$ s and (b) CASE-4: sudden rise in output voltage reference signal at $t = 166.05$ s with proposed controller, (c) unchanged output current in CASE-3 and (d) in CASE-4.

- CASE-1: A sudden rise in VSI output current, $i_{grid}(t)$, at $t = 158.05$ s with unchanged reference signal, $v_{ref}(t)$.
- CASE-2: A sudden fall in VSI output current, $i_{grid}(t)$, at $t = 130.35$ s with unchanged reference signal, $v_{ref}(t)$.
- CASE-3: A sudden fall in output voltage reference signal, $v_{ref}(t)$, at $t = 132.95$ s with unchanged $i_{grid}(t)$.
- CASE-4: A sudden rise in output voltage reference signal, $v_{ref}(t)$, at $t = 166.05$ s with unchanged $i_{grid}(t)$.

The results for CASE-1 and CASE-2 are shown in Fig. 7. It is clearly observed that the output voltage waveforms of VSI, v_C , are insensitive to the sudden changes of i_{grid} (shown

in Fig. 7(c) and Fig. 7(d)) in both CASE-1 and CASE-2 as shown in Fig. 7(a) and Fig. 7(b). Similarly, the results for CASE-3 and CASE-4 are shown in Fig. 8. It is observed that the output voltage waveforms of VSI, v_C , tracks the changes in reference voltage signal, v_{ref} , very quickly as shown in Fig. 8(a) and Fig. 8(b) for both CASE-3 and CASE-4. Moreover, due to constant-current type output loads terminated across the VSI, the output current waveform, i_{grid} is unchanged as shown in Fig. 8(c) and Fig. 8(d). The results shown in Fig. 7 and Fig. 8 clearly substantiate the fact that the dynamic performance of the proposed controller is less sensitive to

transients. Moreover, Table II shows that the reference tracking and harmonic rejection performance illustrated in CHIL results are close enough to the results from SIMULINK/MATLAB. However, due to practical and inevitable limitations like quantization error of ADC of the real controller and efficacy of discretization process, the results may differ slightly but under acceptable limit as evidenced in this case also. Along with the performances, this study also showcases the viability of the proposed $\mathcal{H}_\infty$ -based controller in real low-cost control boards.

V. CONCLUSION

This article demonstrates the design and implementation of robust and optimal single-loop voltage controller for single-phase grid-forming VSI. The model uncertainty of VSI imposed by the unknown changing load is demonstrated and its impact on dynamic model of VSI is shown. $\mathcal{H}_\infty$ -based controller design is introduced to address this issue and the required objectives for the optimal controller are discussed to formulate the optimization problem which leads to final optimal controller. A time-domain SIMULINK-based simulation study substantiates the fact that the resulting controller exhibits superior robustness in performance during varying loading of VSI that conventional multi-loop controller architecture. Moreover, OPAL-RT based CHIL simulations are conducted to verify the viability of the resulting controller.

ACKNOWLEDGMENT

The authors acknowledge Advanced Research Projects Agency-Energy (ARPA-E) for supporting this research through the project titled "Rapidly Viable Sustained Grid" via grant no. DE-AR0001016.

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