

A Novel Power-Hardware-in-the-Loop Interface Method for Grid-Forming Inverter Systems

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Abstract—Power-hardware-in-the-loop (PHIL) simulations of grid-forming (GFM) inverter systems facilitate the testing of drastic scenarios, such as on-grid to off-grid transitions and islanded microgrid operations without a stiff grid. To the authors' best knowledge, most studies in the literature focus on PHIL simulations for grid-following inverter systems. Only a few studies focus on GFM inverters, and those are challenging and problematic, especially for high-power applications. This article proposes a novel PHIL simulation platform that enables interfacing high-power GFM inverter systems. The paper proposes the concept of a virtual GFM inverter as a part of the proposed PHIL interface. This addition of a virtual GFM inverter in the PHIL interface expands the conventional ideal transformer model (ITM) method and enables it to overcome the issues of instability of existing ITM methods. In the validation stage, a PHIL experiment is conducted on a three-phase, 480-V, 125-kVA GFM inverter system with the proposed interfacing method. The results corroborate that the proposed PHIL simulation method performs well and is stable for GFM inverter systems.

Keywords—Droop control, grid forming inverter, ITM-based interface method, power hardware-in-the-loop simulation.

I. INTRODUCTION

To mitigate climate change impacts, renewable energy sources, such as wind and solar, are being increasingly integrated into the current grid. Along with bulk renewable power plants, inverter-based distributed energy resources (DERs), such as photovoltaics and storage, are forming an important part of the grid while potentially increasing grid resilience [1]–[3]. Most DERs are grid-following (GFL) sources, where in voltage across the inverters is set by the grid, and inverters provide power depending on a set point up to the instantaneous capacity; however, the low inertia and uncertainty of DERs can cause unexpected grid stability issue, such as large frequency swings [4]. To address such issues, grid-forming

(GFM) inverters provide viable control strategies by providing frequency damping and microgrid-forming capability under contingency scenarios [5]; however, evaluating the proposed strategy requires extensive studies and experiments of real scenarios. Power-hardware-in-the-loop (PHIL) simulation can be a promising option because it provides an evaluation of physical hardware under test (HUT) with real power flow.

Irrespective of the type of HUT (i.e., GFL or GFM inverters), the configuration of the PHIL simulation itself is challenging. A PHIL simulation consists of a real-time software simulation, the physical inverter HUT and the interface between them; therefore, even when the software simulation and hardware itself are stable individually, an improper interface method between them can lead to the overall instability of the entire system. Moreover, the inaccurate interfacing method may lead to incorrect virtual active and reactive power injections in the simulated system from the HUT. Several interfacing methods have been proposed in the literature. One of the most common solution is the ideal transformer model (ITM) method [6]. Because of its ease of implementation and high accuracy, it is suitable for PHIL simulations of a large, multi-inverter grid; however, it has a problem of a low stability region. The partial circuit duplication (PCD) method increases the region of stability compared to the ITM method [6]; however, this approach requires identical linking impedances to be included in both the simulated and physical systems, which is challenging to ensure in reality.

There exist various works on the PHIL-interface simulations for inverter systems with real-time simulators; however, the majority of the existing works focus on the method of interfacing a GFL inverter [6]–[9] and test the power injection capability under the presence of an emulated grid. But if more drastic scenarios are required to be tested, such as on-grid to off-grid transitions and islanded microgrid operations, PHIL simulations of GFM inverters are required because the operation of GFL inverters relies on the phase-locked loop, which requires an external voltage source with controlled voltage and frequency. To the authors' best knowledge, only a few studies exist in the literature that focus on PHIL simulations of GFM inverters, despite of its importance [10],[11].

This paper is filling the gap by proposing a novel PHIL interface method focused on GFM inverters. This paper proposes

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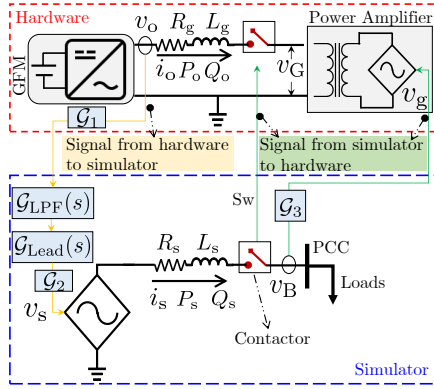


Fig. 1: The PCD-based PHIL interface method for GFM inverter systems as proposed in [10], [11].

the concept of a virtual GFM inverter as part of the proposed PHIL interface. This addition of a virtual GFM inverter in the PHIL interface expands the conventional ITM method and enables it to overcome the issues of the instability of existing ITM methods caused by the lack of stable voltage and frequency of the emulated system. The detailed analysis on the proposed PHIL interface method and the design guidelines for interfacing controllers are provided. A PHIL experiment on three-phase, 480-V, 125-kVA GFM inverter system with the proposed interfacing method corroborates that the proposed method performs well and is stable for GFM inverter system.

II. EXISTING INTERFACE METHOD FOR GFM INVERTERS

In this section, an existing PHIL interface method, as proposed in [10], [11], will be briefly described. By pinpointing the practical challenges of the method, this section will lead to the motivation of the proposed PHIL interface method.

A. Description of the Interface Method

The system under study is a single GFM inverter, connected to a point of common coupling (PCC) via a power line with line inductance, L_g , and line resistance, R_g , in series with a contactor. At the PCC, multiple loads are lumped into one load and are being supplied by the GFM inverter. The corresponding PHIL setup is shown in Fig. 1. Note that the PHIL interface method adopted in [10], [11] is the conventional PCD method.

Inside the “Simulator” (blue dashed box), the GFM inverter is emulated as a controllable voltage source terminated at the PCC via the emulated line parameters, contactor, and supplying the lumped loads. The “Hardware” (red dashed box) includes a physical inverter, operated in grid-forming mode, is connected to a “Power Amplifier.” As the name suggests, the interconnect is via a physical line with inductance, L_s , and resistance, R_s , and a physical contactor. The signals that are sent and received between the Simulator and Hardware are: **From Hardware to Simulator:** Instantaneous voltage waveforms across the physical GFM inverter, v_o , are measured via voltage sensors and sent to the Simulator and fed to the controllable voltage source as input. v_o is processed via $\mathcal{G}_1$, $\mathcal{G}_{LPF}(s)$, $\mathcal{G}_{Lead}(s)$, and $\mathcal{G}_2$, as shown in Fig. 1.

From Simulator to Hardware: Instantaneous voltage waveforms at the PCC, v_B , inside the Simulator, are captured, processed via $\mathcal{G}_3$, and sent to the Hardware and fed back to the Power Amplifier. Also, a digital signal, Sw, is sent to the physical contactor for controlling ON/OFF, as shown in Fig. 1. The purpose of $\mathcal{G}_1$, $\mathcal{G}_2$, $\mathcal{G}_3$, $\mathcal{G}_{LPF}(s)$, and $\mathcal{G}_{Lead}(s)$ are:

- $\mathcal{G}_1$ is the step-down gain of the voltage sensor/potential transformer for voltage measurement in the Hardware.
- $\mathcal{G}_2$ is the step-up gain inside the Simulator to make the signal, v_s , comply with the system under study.
- $\mathcal{G}_3$ is the step-down gain inside the Simulator to make the signal, v_g , comply with the specification of the Power Amplifier of the Hardware.
- $\mathcal{G}_{LPF}(s)$ is a first-order, low-pass filter modeled inside the Simulator. The purpose of the filter is to attenuate any high-frequency components in measured v_o .
- $\mathcal{G}_{Lead}(s)$ is a first-order, phase-lead compensator modeled inside the Simulator. The phase lag introduced by $\mathcal{G}_{LPF}(s)$ causes the injection of a fictitious real and reactive powers inside the Simulator. The purpose of the compensator is to compensate the phase lag.

A stability and trackability study is carried out to show that:

- If $\mathcal{G}_1$, $\mathcal{G}_2$, $\mathcal{G}_3$ are properly selected and $\mathcal{G}_{LPF}(s)$, $\mathcal{G}_{Lead}(s)$ are properly tuned, then $v_o = v_s$ and $v_B = v_g$.
- If $R_g = R_s$, $L_g = L_s$, then $i_o = i_s$, $P_o = P_s$, $Q_o = Q_s$.

B. Challenges of PCD-Based Interface Method

The PCD-based PHIL interface method, as discussed in previous sub-section, poses multiple challenges that are broadly classified into categories and are described in detail as follows:

• Challenges in Hardware Side : Challenges are:

i) The PCD-based PHIL interface approach requires the linking impedance to be included in both simulated (i.e., inside Simulator of Fig. 1) and physical systems (i.e., inside Hardware of Fig. 1). The physical impedance should be capable of handling at least the fully rated current of the GFM inverter under study; therefore, the need to include this impedance in the Hardware could be problematic, especially for high-power applications [12].

ii) To have a perfect match in the Hardware and Simulator of Fig. 1 (i.e., $i_o = i_s$, $P_o = P_s$, $Q_o = Q_s$), R_g and L_g of the physical impedance in Hardware should match the emulated R_s and L_s of Simulator. This could be challenging in practice because of the inevitable design error of a physical inductor and resistors.

• Challenges in Software Side : Challenges are:

i) A proper PHIL interface requires modeling multiple elements used in the system, e.g., a model of a delay imposed by the voltage sensor/potential transformer, power amplifier, and analog-to-digital and digital-to-analog converter module. Altogether, these models generate a significant amount of delay in the closed loop and could potentially impact system stability [13]. The premise of this method is idealistic and does not account for these models in the design.

ii) This method assumes that v_G perfectly tracks v_g in Fig. 1. However commercially available power amplifiers usually impose an inherent delay between the input control signal,

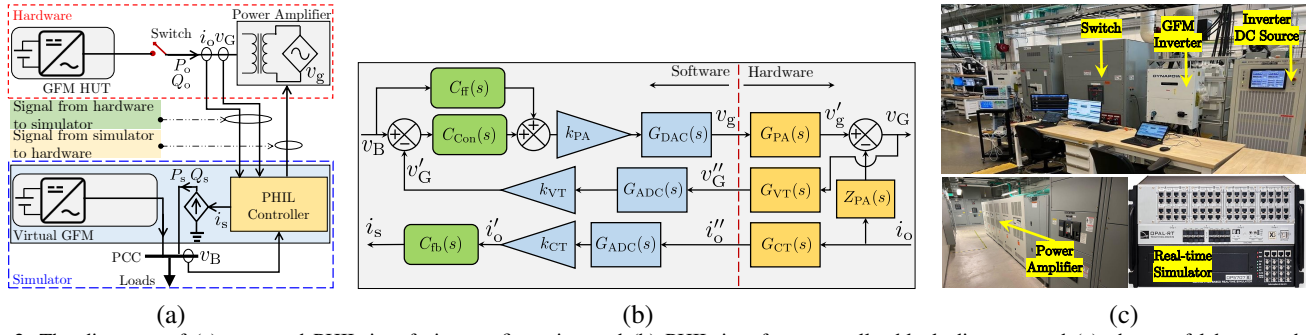


Fig. 2: The diagrams of (a) proposed PHIL interfacing configuration and (b) PHIL interface controller block diagram, and (c) photos of laboratory-based experimental setup by NREL.

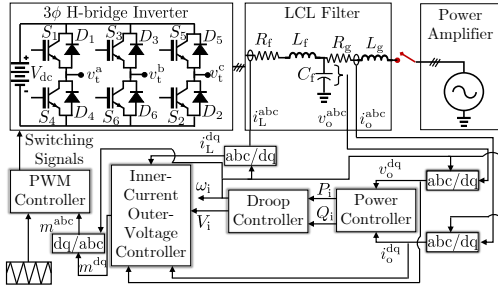


Fig. 3: Power circuit and control loops of virtual and physical GFM inverter.

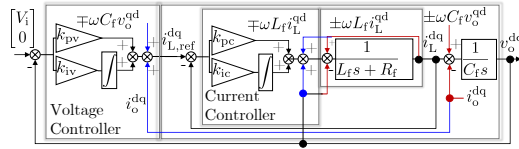


Fig. 4: Inner-current-outer-voltage controller for GFM inverter systems.

v_g , and the output power signal, v_G . It is hence recommended to use an additional regulator to enhance the concerned tracking performance. This method does not account for these regulator designs.

III. PROPOSED INTERFACE METHOD

A. Proposed Virtual GFM-Based PHIL Interface

To overcome the challenges of the PCD-based PHIL interface method, this paper proposes an ITM-based extended PHIL interface method that is suitable for testing GFM inverters. Conventional ITM methods have a small stability region and often lead to instability of the entire system. In the proposed method, like the conventional ITM method, a physical GFM inverter, “GFM HUT”, is connected to a Power Amplifier without linking impedance in the Hardware side, as shown in Fig. 2(a). Also, on the Simulator side, a GFM inverter is emulated as a controllable voltage source, called a “Virtual GFM”, connected to the PCC without emulated line parameters. This can also be seen as moving one GFM inverter of a large system under test into the simulation side. The power circuit of both the virtual and the physical GFM inverter system is terminated via a LCL filter, with L_f , C_f , and R_f as filter inductance, capacitance, and parasitic resistance, respectively, as shown

in Fig. 3. A dq-frame multi-loop controller is employed that generates the modulated voltage vector signal, m^{abc} , to the pulse-width modulation (PWM) controller to generate the switching signals, resulting in the terminal voltages, v_t^a , v_t^b , and v_t^c . This multi-loop control consists of a conventional inner-current-outer-voltage controller, as discussed in [14] and as shown in Fig. 4. By referring to Fig. 3, the power and the droop controller are discussed briefly:

1) *Power Controller*: The dq component of output voltage, v_o^{dq} , and current, i_o^{dq} , are used to determine the instantaneous active power, p_i , and reactive power, q_i , of the GFM inverter and processed through low-pass filters with the time constant, $\tau_s \in \mathbb{R}_{>0}$, to obtain the average active power, $P_i = [1/(\tau_s s + 1)]p_i$, and reactive power, $Q_i = [1/(\tau_s s + 1)]q_i$, where $p_i := 1.5 \times [v_{o,i}^d i_{o,i}^d + v_{o,i}^q i_{o,i}^q]$ and $q_i := 1.5 \times [v_{o,i}^q i_{o,i}^d - v_{o,i}^d i_{o,i}^q]$.

2) *Conventional Droop Controller*: The conventional active power/frequency, P-f, and reactive power/voltage, Q-V, droop control law is described as $\omega_i = \omega_N - n_P P_i$, and $V_i = V_N - m_Q Q_i$, where, ω_N , V_N are the nominal frequency (in rad/s) and voltage (in volt) of the system respectively. n_P and m_Q are the P-f and Q-V droop coefficients respectively. The values of n_P and m_Q are typically chosen such that ω_i and V_i are within the allowed specification, defined by IEEE 1547 [15], and the GFM is at the rated loading condition.

The virtual GFM inverter is modeled close to the physical GFM inverter with the same droop gains and similar response time. The following remarks are made in conclusion:

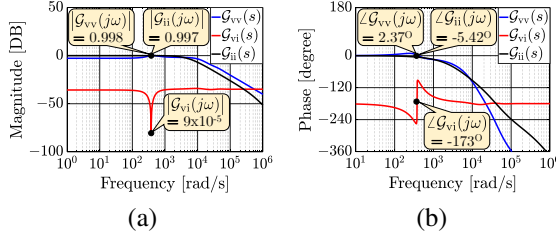
Remark 1: ITM method-based interfacing of the physical GFM inverter, modeled as a current source, and the Power Amplifier, modeled with only passive load, inside the Software side is challenging. Small disturbances in the current source model of the ITM-interfaced model of the physical GFM inverter results in significant disturbances in the voltage across the grid simulator that lead to instability. To overcome this, the virtual GFM inverter is included in the Software side, as shown in Fig. 2(a).

Remark 2: The virtual GFM is modeled close to the physical GFM inverter. This provides a stable and accurate PHIL-based hardware testing and validation, however, it is not mandatory to have a similar virtual GFM model in this proposed method.

Remark 3: Unlike the existing PCD-based approach, the proposed method does not require a linking impedance, which enables it to be more suitable for testing the high-power simulation. As a result, the proposed approach overcomes the

TABLE I: SYSTEM MODELING FOR PHIL INTERFACE CONTROLLER

Element	Model
T_s	$50 \mu s$
$G_{PA}(s)$	$e^{-sT_s} \times 2\pi 1950 / [s + 2\pi 1950]$
$Z_{PA}(s)$	$4.5 \times 10^{-5} s + 0.018$
$G_{VT}(s)$	$e^{-sT_s} \times [2\pi 14 \times 10^3] / [s + 2\pi 14 \times 10^3]$
$G_{CT}(s)$	$e^{-sT_s} \times [2\pi 100 \times 10^3] / [s + 2\pi 100 \times 10^3]$
$G_{ADC}(s), G_{DAC}(s)$	$e^{-sT_s} \approx [1 - (T_s/2)s] / [1 + (T_s/2)s]$
k_{PA}, k_{VT}, k_{CT}	$1/42, 82.41, 30.76$
$C_{Con}(s) [\omega = 2\pi 60]$	$0.1 + \frac{200 \times 2\zeta\omega s}{s^2 + 2\zeta\omega s + \omega^2}, \zeta = 1/\omega$
$C_{ff}(s)$	0.7
$C_{fb}(s)$	$2\pi 800 / [s + 2\pi 800]$

Fig. 5: Bode plot of (a) magnitude and (b) phase of $G_{vv}(s)$, $G_{vi}(s)$ and $G_{ii}(s)$.

challenges in the hardware side, as mentioned in Section II.

B. ITM-Based PHIL Interface Controller Synthesis

The ITM-based PHIL interface control system has the PCC voltage, v_B , and measured current at the output of the power amplifier, i_o , as the input reference signals, the voltage at the output of the power amplifier, v_G , and the PHIL equivalent current signal, i_S , as the output variables to be primarily controlled by three compensators, $C_{Con}(s)$, $C_{ff}(s)$, and $C_{fb}(s)$, as shown in Fig. 2(b). The plant models are described as follows:

- 1) $G_{PA}(s)$ is the power amplifier's transfer function, and $Z_{PA}(s)$ is the output impedance of the power amplifier.
- 2) $G_{VT}(s)$ and $G_{CT}(s)$ are the transfer functions representing the voltage and current sensors, respectively.
- 3) $G_{ADC}(s)$ and $G_{DAC}(s)$ are the transfer functions representing the analog-to-digital (A/D) and digital-to-analog (D/A) conversion delays, respectively.
- 4) $k_{PA}(s)$, $k_{VT}(s)$, and $k_{CT}(s)$ are the corresponding voltage step-down and voltage and current step-up gains required between the emulated and physical systems, respectively.

Compensators are required to be designed to achieve: 1) the closed-loop PHIL system must be internally stable, 2) v_G should track its reference signal, v_B , 3) i_S should track its reference signal, i_o . The proper tunings of the feedback compensator, $C_{Con}(s)$, and the feed-forward compensator, $C_{ff}(s)$, are required to achieve the first and second objectives, whereas the tuning of the current compensator, $C_{fb}(s)$, is required to achieve the last objective. The detailed tuning process is out of scope of this work, and can be found in [13]. The classical stability margin-based controller tuning is used with enough phase and gain margin, and the resulting controllers for the system under study are given in Table I. The resulting multi-input, multi-output (MIMO) closed-loop

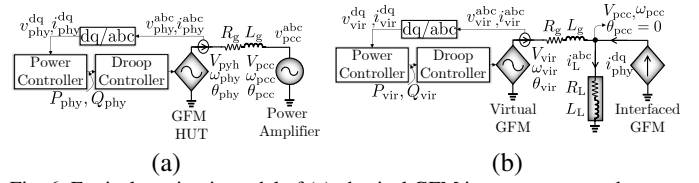


Fig. 6: Equivalent circuit model of (a) physical GFM inverter connected across the power amplifier, (b) virtual GFM inverter connected across ITM-based modelled GFM inverter with emulated load.

system is:

$$\begin{bmatrix} v_G(s) \\ i_S(s) \end{bmatrix} = \begin{bmatrix} G_{vv}(s) & G_{vi}(s) \\ G_{iv}(s) & G_{ii}(s) \end{bmatrix} \begin{bmatrix} v_B(s) \\ i_o(s) \end{bmatrix}, \text{ where}$$

$$G_{vv}(s) = \frac{G_{PA}(s)G_{DAC}(s)k_{PA}C_{Con}(s) + C_{ff}(s)}{1 + G_{PA}(s)G_{DAC}(s)k_{PA}K_{VT}G_{ADC}(s)G_{VT}(s)},$$

$$G_{vi}(s) = \frac{-G_{PA}(s)G_{DAC}(s)k_{PA}Z_{PA}(s)}{1 + G_{PA}(s)G_{DAC}(s)k_{PA}K_{VT}G_{ADC}(s)G_{VT}(s)},$$

$$G_{iv}(s) = 0, \text{ and } G_{ii}(s) = C_{fb}(s)k_{CT}G_{ADC}(s)G_{CT}(s).$$

The Bode diagrams of $G_{vv}(s)$, $G_{vi}(s)$ and $G_{ii}(s)$ are shown in Fig. 5(a) and Fig. 5(b). From the magnitude and phase response of the MIMO transfer functions, it can be concluded that the compensators ensure $v_G(s) \approx v_B(s)$ and $i_S(s) \approx i_o(s)$ with minimal magnitude and phase tracking error.

C. Analysis of the Proposed ITM Method-Based PHIL Interfacing of Physical Inverter with Virtual GFM Inverter

For ease in analyzing, the model of the individual inverter will be developed with the followings considerations:

- The inner-current-outer-voltage control loop is stable and has faster (> 10 times) dynamics compared to the power and droop controller and tracks its voltage reference with minimal (assumed zero) tracking error, as suggested in [14].
- The power amplifier is a voltage source with voltage, V_{pcc} , and frequency, ω_{pcc} , and the load is a Z-type load [16].
- The compensators have negligible tracking errors in the ITM-based interfacing approach, mentioned in Section III.B.
- All abc-dq conversions are adopted w.r.t. a common reference, with phase angle, θ_{pcc} , and frequency, ω_{pcc} .

This allows for modeling the physical and virtual GFM inverters as a voltage source with controllable phase, frequency, and amplitude, as shown in Fig. 6(a) and Fig. 6(b). Now, the physical GFM inverter terminated across the power amplifier can be modeled by the following nonlinear system equations:

$$\dot{\theta}_p = \omega_{phy} - \omega_{pcc}, \text{ where } \theta_p := \theta_{phy} - \theta_{pcc}, \quad (1)$$

$$\tau_S \dot{\omega}_{phy} = \omega_N - \omega_{phy} - n_P p_{phy}, \quad (2)$$

$$\tau_S \dot{V}_{phy} = V_N - V_{phy} - m_Q q_{phy}, \quad (3)$$

$$L_g \dot{i}_{phy}^d = V_{phy} \cos \theta_p - R_g i_{phy}^d - v_{pcc}^d + \omega_{ref} L_g i_{phy}^q, \quad (4)$$

$$L_g \dot{i}_{phy}^q = V_{phy} \sin \theta_p - R_g i_{phy}^q - v_{pcc}^q - \omega_{ref} L_g i_{phy}^d, \quad (5)$$

where θ_{phy} is the phase angle of the physical GFM inverter w.r.t. the PCC, and $p_{phy} := 1.5[V_{phy}i_{phy}^d \cos \theta_p + V_{phy}i_{phy}^q \sin \theta_p]$, and $q_{phy} := 1.5[-V_{phy}i_{phy}^d \sin \theta_p + V_{phy}i_{phy}^q \cos \theta_p]$. This results in a 5th-order nonlinear electro-magnetic model for the physical GFM inverter. Similarly, the

virtual GFM inverter terminated across the load and the ITM-based model of the physical GFM inverter can be modeled by the following nonlinear system equations:

$$\dot{\theta}_v = \omega_{vir} - \omega_{pcc}, \text{ where } \theta_v := \theta_{vir} - \theta_{pcc}, \quad (6)$$

$$\tau_S \dot{\omega}_{vir} = \omega_N - \omega_{vir} - n_P p_{vir}, \quad (7)$$

$$\tau_S \dot{V}_{vir} = V_N - V_{vir} - m_Q q_{vir}, \quad (8)$$

$$L_g \dot{i}_{vir}^d = V_{vir} \cos \theta_v - R_g i_{vir}^d - v_{pcc}^d + \omega_{ref} L_g i_{vir}^q, \quad (9)$$

$$L_g \dot{i}_{vir}^q = V_{vir} \sin \theta_v - R_g i_{vir}^q - v_{pcc}^q - \omega_{ref} L_g i_{vir}^d, \quad (10)$$

where θ_{vir} is the phase angle of the physical GFM inverter w.r.t. the PCC, and $p_{vir} := 1.5[V_{vir} i_{vir}^d \cos \theta_p + V_{vir} i_{vir}^q \sin \theta_p]$, and $q_{vir} := 1.5[-V_{vir} i_{vir}^q \cos \theta_p + V_{vir} i_{vir}^d \sin \theta_p]$. This results in a 5th-order nonlinear electromagnetic model for the virtual GFM inverter. Now, using the Kirchhoff's Current Law at the PCC, the following equations are derived for the load:

$$L_L \dot{i}_L^d = v_{pcc}^d - R_L i_L^d + \omega_{ref} L_L i_L^q, \text{ where, } i_L^d = i_{phy}^d + i_{vir}^d,$$

$$L_L \dot{i}_L^q = v_{pcc}^q - R_L i_L^q - \omega_{ref} L_L i_L^d, \text{ where, } i_L^q = i_{phy}^q + i_{vir}^q.$$

As a result, the entire system can be modeled by a nonlinear system, $\dot{\underline{x}} = \underline{G}(\underline{x})$, where $\underline{G}(\cdot)$ consists of (1)–(10) and the load model. Here, $\underline{x}^\top = [\theta_p \ \theta_v \ \omega_{phy} \ \omega_{vir} \ V_{phy} \ V_{vir} \ i_{phy}^d \ i_{vir}^d \ i_{phy}^q \ i_{vir}^q]$. As a result, the complete system is a 10th-order nonlinear autonomous system with state vector $\underline{x}$. The following remarks are made:

- In steady state, (1) and (5) yield $\omega_{phy} = \omega_{vir} = \omega_{pcc}$, which implies $n_P P_{phy} = n_P P_{vir}$, which yields $P_{phy} = P_{vir}$. This is aligned with the conventional findings of the active power sharing capability of multiple droop-based GFM inverters [17].
- It is known that the reactive power sharing accuracy with Q-V droop control is strongly affected by line parameters [18], thus, if line parameters are neglected, then (4), (5) and (9), (10) yield $V_{phy} = V_{vir}$. Hence, it can be stated that $m_Q Q_{phy} = m_Q Q_{vir}$, which yields $Q_{phy} = Q_{vir}$ [17].
- Note here that the assumption of neglecting line impedances is not realistic, and therefore there will be a mismatch in the reactive sharing between GFM inverters.

IV. RESULTS

The PHIL experiment configuration of Fig. 2(a) is used to evaluate a three-phase, 125-kVA, four-quadrant GFM inverter manufactured by Dynapower with Aerovironment AV-900 battery energy storage system, interconnected at the PCC of Fig. 2(a). Each phase of the HUT is interconnected to the appropriate phase using an independent version of the single-phase configuration shown in Fig. 2(b). The PHIL interface consists of the following:

- 1) A three-phase 270-kVA Ametek RS-series power amplifier;
- 2) Three LEM DVL750 voltage transducers;
- 3) A set of three LEM LF-350-S current transducers.

An Opal RT OP5700-series real-time simulator with a time step of $T_s = 50 \mu s$ is used to execute the in-the-loop system, which consists of a bunch of P - Q loads, and the proposed PHIL interface blocks consists of the proposed virtual GFM inverter model and three discrete-time PHIL interface compensators. The parameters of the controller and the power circuit of the virtual and the physical HUT inverter are tabulated in Table II. The experimental setup is shown in Fig. 2(c).

TABLE II: PARAMETERS OF THE VIRTUAL AND HUT INVERTER

Inverter	Value
Ratings (3- ϕ)	480 V (L-L), 60 Hz, 125 kVA
Parameters	$V_{dc} = 850$ V, $f_{sw} = 10$ kHz
Filter	$L_f = 150$ μ H, $L_g = 15$ μ H, $C_f = 110$ μ F
Control	Value
Droop Gains	$0.5/125$ Hz.MW ⁻¹ , $24/125$ V.kVA ⁻¹
Power Control	Virtual [$\tau_S=10$ ms], HUT [$\tau_S=1$ ms]
Voltage Control	Virtual [$k_{pv}=2$, $k_{iv}=3$], HUT [$k_{pv}=7$, $k_{iv}=50$]
Current Control	Virtual [$k_{pc}=1$, $k_{ic}=1$], HUT [$k_{pi}=0.1$, $k_{iv}=20$]

TABLE III: PERFORMANCE OF THE PHIL INTERFACE METHOD

Zone	P _{Error} [%]			Q _{Error} [%]		
	Max[+]	Max[-]	Avg	Max[+]	Max[-]	Avg
Zone-1	1.85	-1.88	0.08	5.79	-3.30	0.78
Zone-2	2.28	-2.64	0.09	4.85	-4.97	1.24
Zone-3	3.70	-3.46	0.23	8.59	-4.47	2.25
Zone-4	4.03	-2.93	0.35	11.23	-4.09	3.46
Zone-5	3.78	-2.81	0.72	10.76	-3.92	4.78

A. Experimental Validation and Results

In this experiment, four events of load jump are conducted to validate the performance of the proposed PHIL interface method: (a) Event 1: a jump from 0-kVA to 50-kVA load, (b) Event 2: a jump from 50-kVA to 100-kVA load, (c) Event 3: a jump from 100-kVA to 150-kVA load and, (d) Event 4: a jump from 150-kVA to 200-kVA load, with a power factor of 0.9 lagging. Fig. 7(a), 7(b), and 7(c) show the performance of the PHIL interface controller of Fig. 2(b) followed in this experiment inside a particular time window. For the discrete-time PHIL interface compensators, the reference signals are v_{PHIL}^a , v_{PHIL}^b and v_{PHIL}^c . The corresponding scaled voltages measured at the analog input port of the real-time simulator are v_{Meas}^a , v_{Meas}^b , and v_{Meas}^c . The instantaneous voltage error in percentage is defined as $v_{Error}^a[\%] := 100 \times (v_{PHIL}^a - v_{Meas}^a)/v_{rated}^a$, $v_{Error}^b[\%] := 100 \times (v_{PHIL}^b - v_{Meas}^b)/v_{rated}^b$, and $v_{Error}^c[\%] := 100 \times (v_{PHIL}^c - v_{Meas}^c)/v_{rated}^c$. Reasonably good tracking performances of the PHIL interface compensators are observed in Fig. 7(a), 7(b), and 7(c). The maximum and minimum instantaneous tracking errors in all three phases during the entire experiment are bound under ± 2 V which is approximately $\pm 0.5\%$.

Fig. 8(a) and Fig. 8(b) show the performance of the active and reactive power sharing performance between the virtual GFM as a part of the proposed PHIL interface, $P_{Virtual}$ and $Q_{Virtual}$, and the ITM-based equivalent PHIL model of the HUT, P_{PHIL} , Q_{PHIL} , for given loading conditions with P_{Load} and Q_{Load} . As observed in Fig. 8(a), the active power sharing performance is better than the reactive power sharing performance, as shown in Fig. 8(b). Note that the reactive power sharing is affected by the equivalent unequal line parameters and inevitable tracking errors of the PHIL interface controllers. The robustness of the PHIL controllers is usually recommended for better performance, as suggested by [13]; however, this discussion is out of scope of this work. Fig. 8(c) and Fig. 8(d) show the performance of the power tracking capability of the PHIL interface controller by showing the active and reactive power output of the ITM-based equivalent PHIL model of the HUT, P_{PHIL} , Q_{PHIL} , and of the real HUT, P_{HUT} , Q_{HUT} . As observed, the active and reactive power tracking

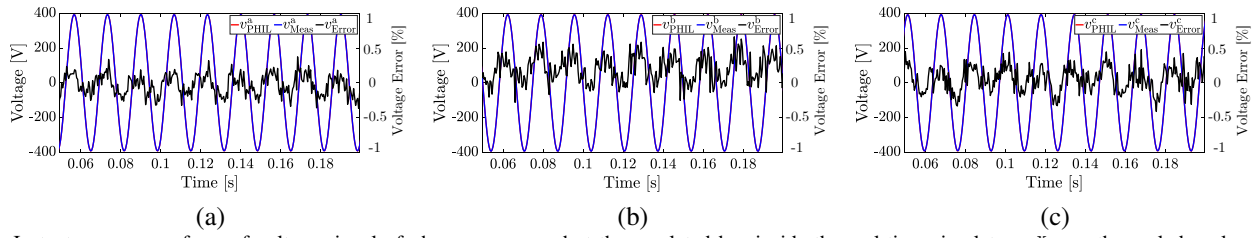


Fig. 7: Instantaneous waveform of voltage signal of phase x measured at the emulated bus inside the real-time simulator, v_{PHIL}^x , the scaled analog voltage measured at analog input port of the real-time simulator, v_{Meas}^x , and the error in percentage, respectively where x is (a) phase A, (b) phase B, (c) phase C.

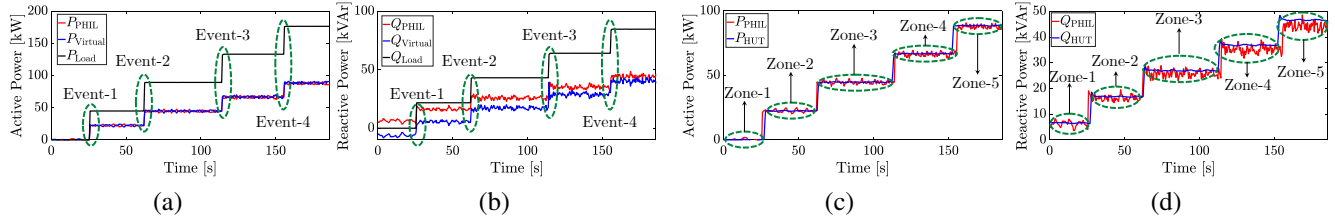


Fig. 8: Experimental results during events 1-4 of: (a) active power output and (b) reactive power output of the virtual GFM inverter, PHIL-interfaced model of the HUT, and the total load in the system, and (c) active power and (d) reactive power of the PHIL-interfaced model and the HUT, respectively.

capability of the PHIL interface controller are qualitatively well, and Table III provides the quantitative numbers of the performance, where $P_{Error} = [P_{HUT} - P_{PHIL}]/P_{HUT}$ and $Q_{Error} = [Q_{HUT} - Q_{PHIL}]/Q_{HUT}$.

V. CONCLUSION AND FUTURE WORK

This article proposes a novel PHIL simulation platform that enables interfacing high-power GFM inverter systems. By proposing the concept of a virtual GFM inverter as part of the PHIL interface for a GFM inverter, the paper expands the conventional ITM method and enables it to overcome the existing issues of instability. Results in the high-power PHIL validation stage corroborate the fact that the proposed PHIL simulation method performs well and is stable for GFM inverter systems. The authors have identified the potential of this method for the application of PHIL simulations by interfacing an entire high-power physical microgrid hardware system consisting of multiple inverter systems and loads with a simulated microgrid in a real-time platform. This will be part of future research works.

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